UM_APIX2_ADK_TX (Rev2)

Order ID: UM_APIX2_ADK_TX
March 2015
Revision 1.2_A1

APIX2 ADK Transmitter Board (Rev2)

1.0 Introduction

The APIX2 ADK Transmitter board provides a variety of data inputs for digital video, audio and control data processing to demonstrate all main functions of APIX2 INAP375T Transmitter devices. All board functions can be controlled via a software GUI to an on-board microcontroller. Furthermore all functional pins of the INAP375T device and board controls are accessible via pin headers

Features:

- Two independent HDMI/ DVI ports for digital video input (24Bit or 18 Bit width color depth)
- HSD or MX49 connector for APIX2 serial port
- USB Interface to software GUI for easy control of all board functions
- HDMI Audio input processing
- Power over APIX support

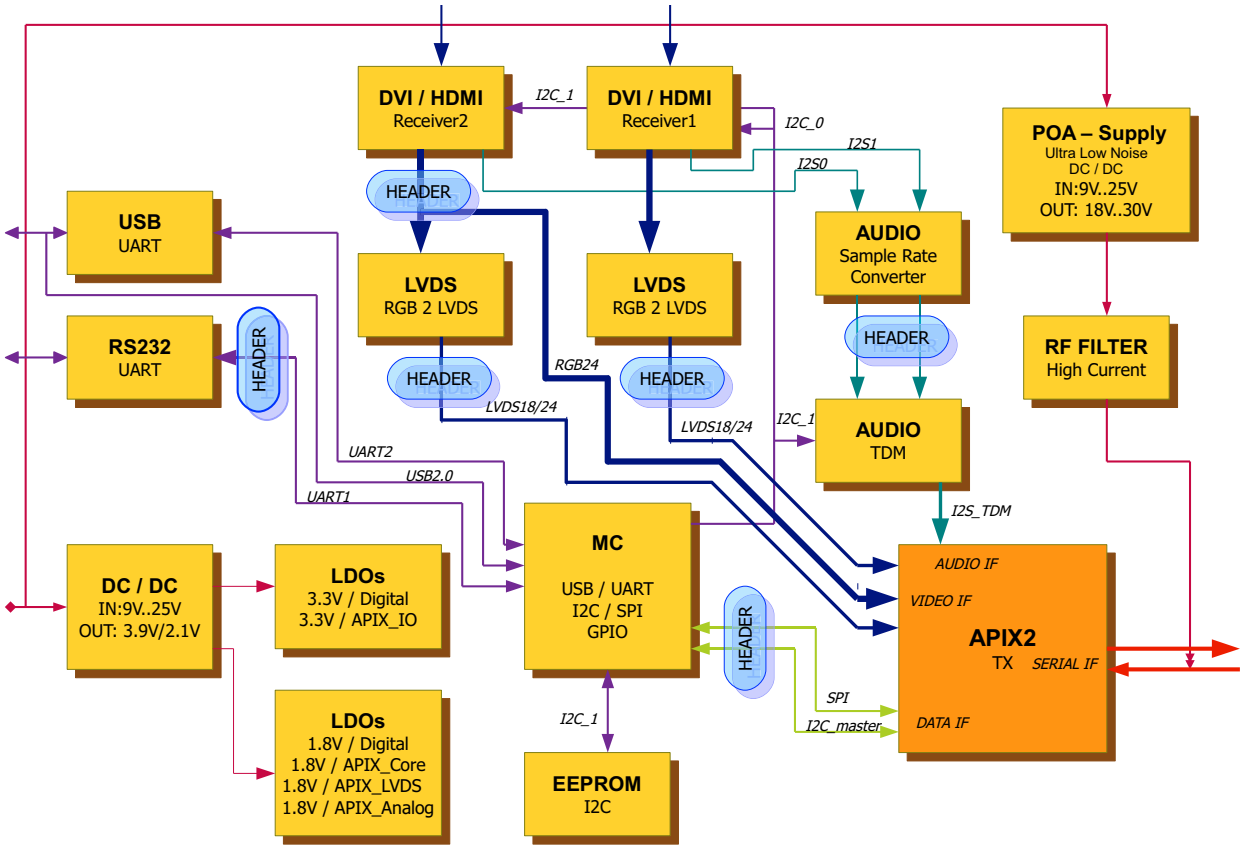


Figure 1-1: Tx Application Board - Block Diagram

Table of Contents

List of Tables

List of Figures

2.0 Functional description

2.1 Video path

The APIX2 ADK Transmitter board offers video input from two independent HDMI/DVI sources. Both HDMI/DVI inputs are converted to parallel RGB data (24 Bit color depth). The parallel RGB signals are converted to 3-lane (18Bit) or 4-lane (24Bit) LVDS video streams which are fed directly into the INAP375T transmitter device. Alternatively 24Bit RGB data can be fed to the APIX pixel interface (assembly option).

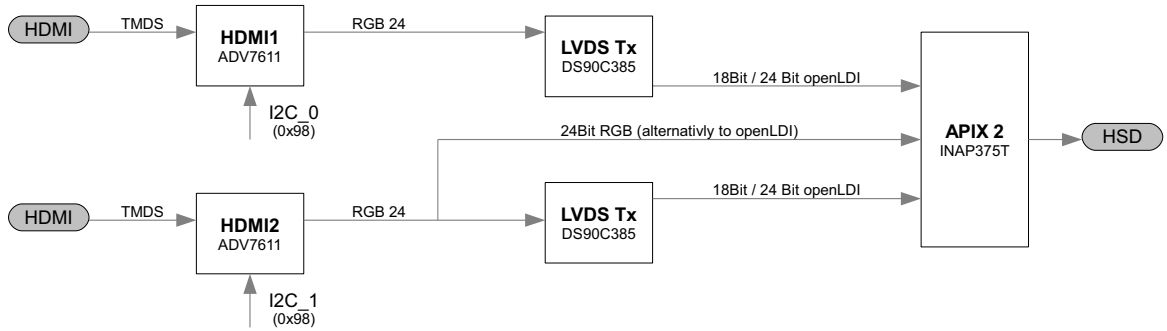


Figure 2-1: APIX2 ADK Transmitter video path

All control functions as well as EDID informations of both HDMI/DVI devices can be controlled via I2C bus from the on-board microcontroller.

2.2 Audio path

Audio information is taken from the HDMI/DVI streams. Audio data is processed via an ADC and a sample rate converter to I2S TDM digital audio format and routed via the I2S input interface of the INAP375T device.

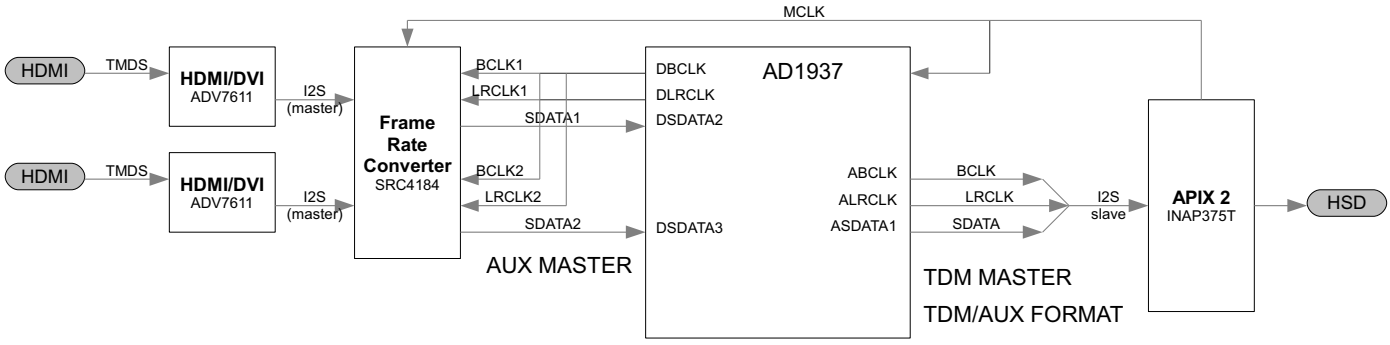


Figure 2-2: APIX2 ADK Transmitter audio path

Alternatively (assembly option) the I2S interface of one HDMI/DVI receiver can be directly fed to the APIX I2S interface to support 7.1 audio formats.

2.3 Control path

All board functions are controlled via on-board microcontroller. The microcontroller is accessible via a software GUI. For more information please refer to the APICO software user manual.

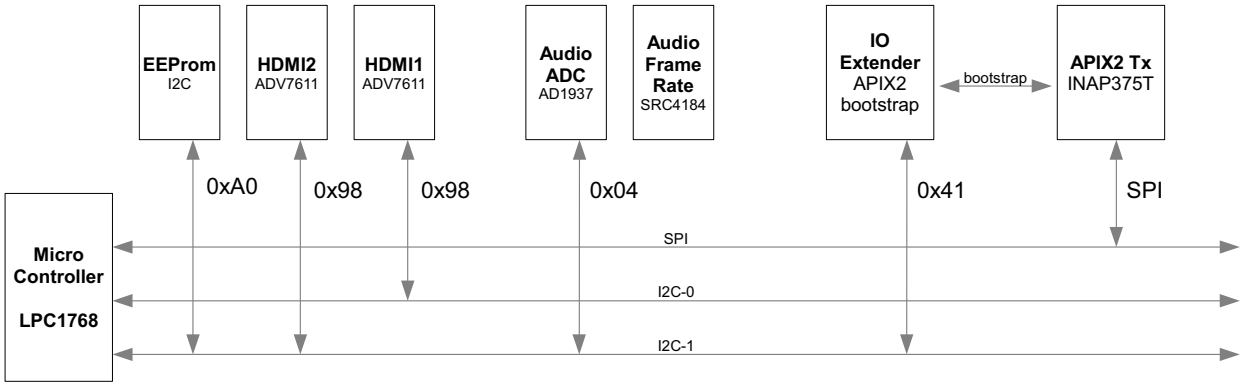


Figure 2-3: APIX2 ADK Transmitter control path

The microcontroller offers two independent I2C busses as well as one SPI bus. The I2S busses manage EDID information and control functions of both HDMI/DVI devices as well as control functions of the audio analog to digital converter. The SPI bus manages configuration of the INAP375T Transmitter device and the settings of the audio frame rate converter.

The setting of the bootstrap pins of the INAP375T device (for more information please refer to the data sheet) can be controlled by an I/O extender which is accessible via I2C-1 (see chapter 2).

The microcontroller‘s connections to the INAP375T device can be tri-stated via dip switch (see chapter 3.3).

3.0 Hardware description

3.1 Board connectors

3.1.1 Standard connectors and interfaces

- 2 HDMI connectors for video input
- 1 USB2.0 connector for interfacing the boards's µC to the PC
- 1 RS232 for ISP (In Circuit Programming) of the µC
- Single 9V..18V (Typ. 12V) DC power supply input to generate all board supplies
- APIX Serial High Speed Interface with either Rosenberger HSD or Molex MX49 connector

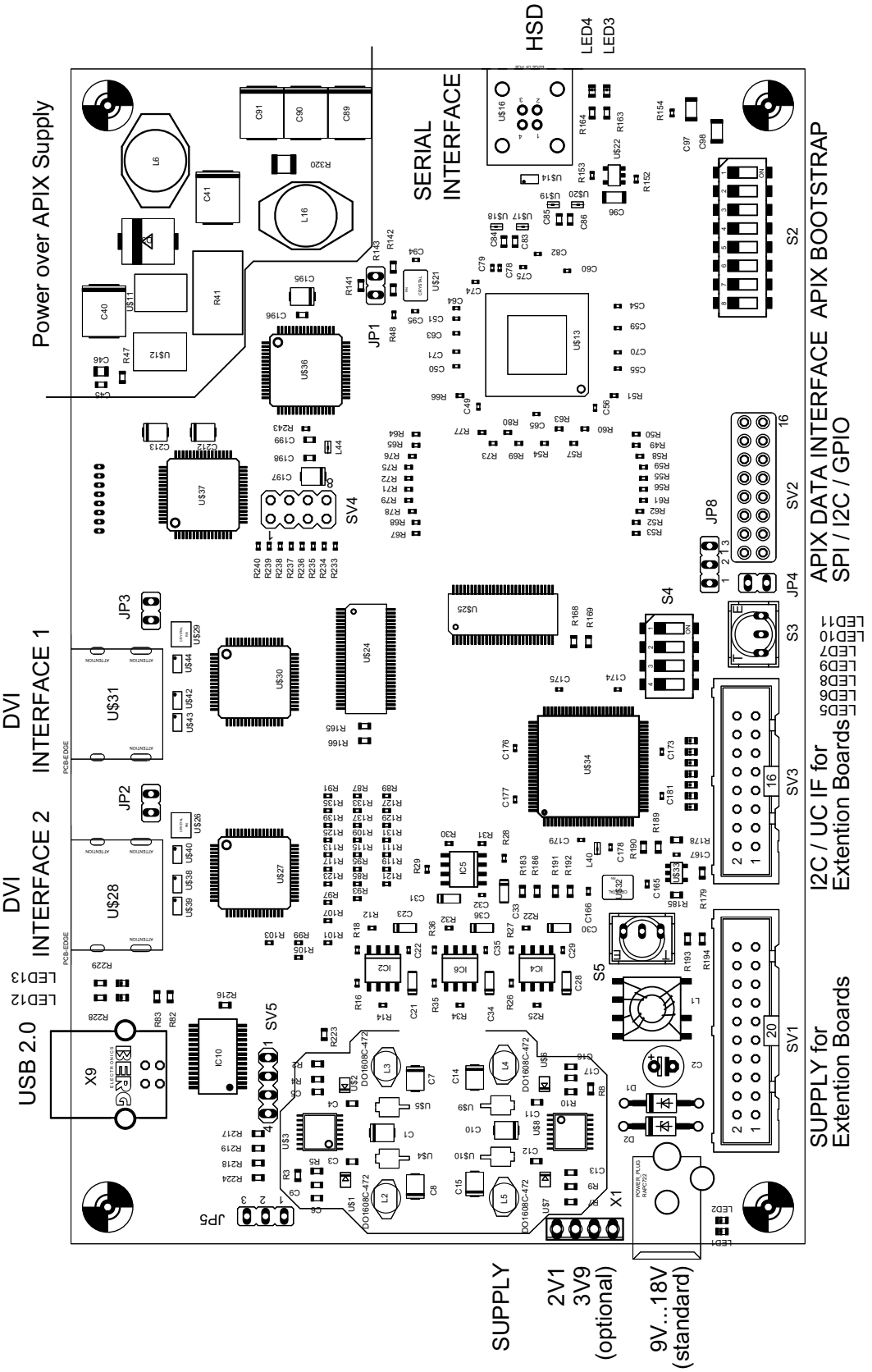
3.1.2 Connectors and interfaces for bench setups

- Direct power supply input to all LDOs (3.9V and 2.1V) allows to disable all DC/DC switcher (EMI tests)
- UART interface alternatively to USB2.0 with 3.3V supply to hook up a POF module (EMI tests)
- APIX I2S audio interface on pin header
- APIX SPI slave interlace on pin header
- APIX I2C interlace on pin header
- APIX GPIO interlace on pin header
- 2 Stereo audio line in
- µC JTAG interface
- µC MII interlace

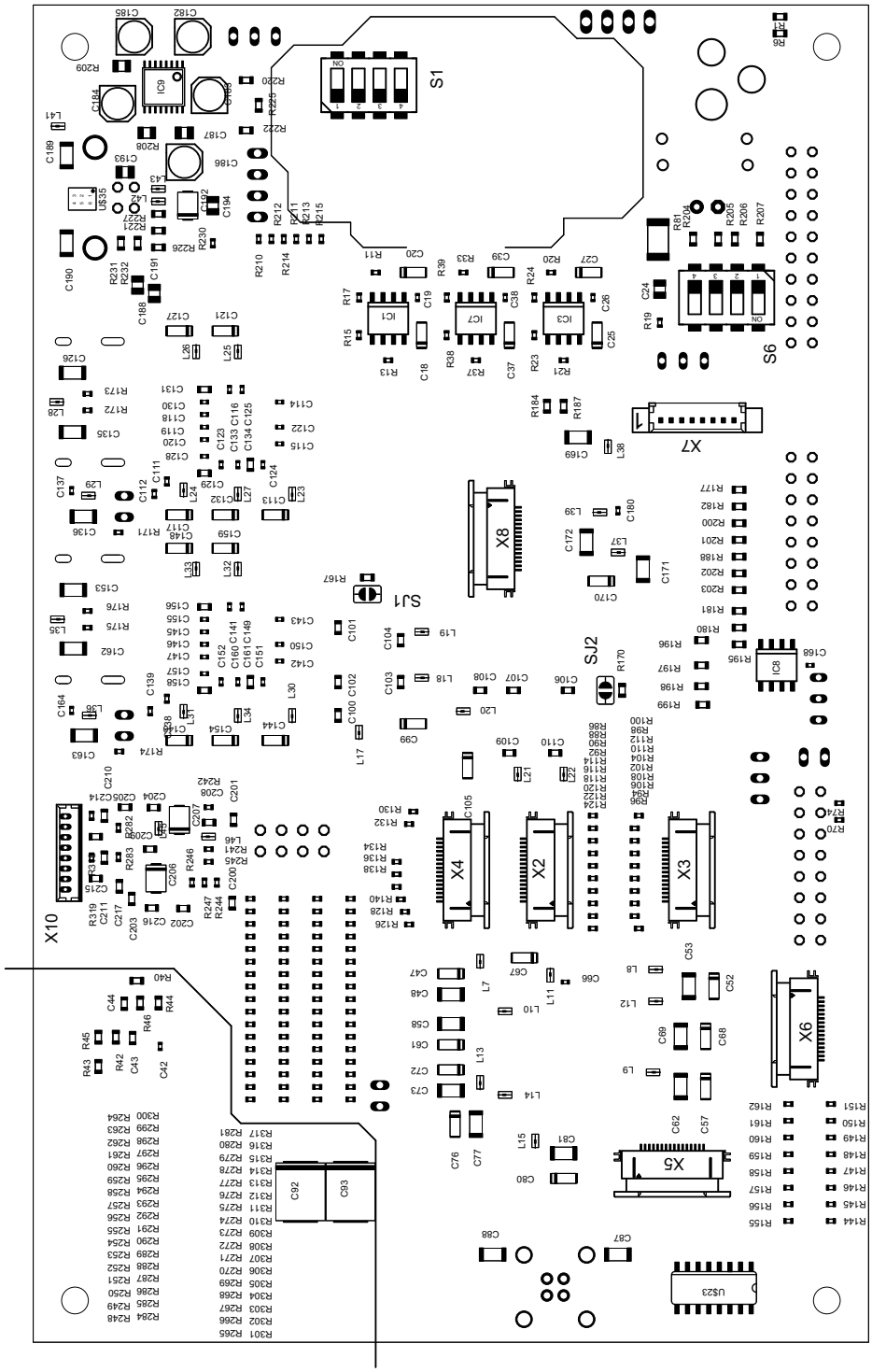
3.1.3 Connectors and interfaces to expansion boards

- APIX pixel interface
- APIX data interface
- 12V, 3.3V and 1.8V power supply
- µC ports
- I2C_0 and I2C_1 bus (from µC)

3.1.4 Top Side


Power over APIX Supply
SERIAL INTERFACE
HSD
LED4
LED3
APIX DATA INTERFACE APIX BOOTSTRAP
SPI / I2C / GPIO
I2C / UC IF for Extention Boards
SUPPLY for Extention Boards
DVI INTERFACE 1
DVI INTERFACE 2
USB 2.0
SUPPLY
2V1
3V9 (optional)
9V...18V (standard)
JP1
JP2
JP3
JP4
JP5
JP8
SV1
SV2
SV3
SV4
SV5
S2
S3
S4
S5
X1
X9

3.1.5 Bottom Side



3.1.6 Connector and interface pin description

JP5	ISP UART Interface	
Pin	**Signal**	**Description**
1	RXD1	Receive data for ISP
2	TXD1	Transmit data for ISP
3	GND	Signal ground

Table 3-1: ISP UART Interface

SV1	Power supply for extension boards	
Pin	**Signal**	**Description**
1,3,5,7,9, 11,13,15, 17,19	GND	Signal ground
2,4	12V0	9V - 18V for extension board's DC/DC converter
14,16	DCDC_3V9	3.9 V Supply for extension board's 3.3V LDOs
18,20	DCDC_2V1	2.1 V Supply for extension board's 1.8V LDOs

Table 3-2: Extension board supply

SV2	APIX2 I2C, SPI slave and GPIO interface	
Pin	**Signal**	**Description**
2,4,6,8,10 ,12,14,16	GND	Signal ground
1	AX_I2C_SCL	APIX2 I2C master interface
3	AX_I2C_SD	

Table 3-3: APIX2 I2C, SPI slave and GPIO interface

SV2	APIX2 I2C, SPI slave and GPIO interface	
Pin	**Signal**	**Description**
5	AX_SPIS_CS2#	APIX2 SPI slave and GPIO interface. Monitor only if µC access is enabled (default). To disable µC access to this signals switch on DIP switch S4.1
7	AX_SPIS_SCK	
9	AX_SPIS_SDI	
11	AX_SPIS_SDO	
13	AX_GPIO_1	
15	AX_GPIO_0	

Table 3-3: APIX2 I2C, SPI slave and GPIO interface

SV3	µC interface for extension boards	
Pin	**Signal**	**Description**
1	UC_P1_25	µC ports for extension boards
2	UC_P2_13	
3	UC_P1_24	
4	UC_P2_12	
5	UC_P1_23	
6	UC_P0_24	
7	UC_P1_22	
8	UC_P0_23	
9	UC_P1_21	
10	UC_P0_22	
11	DIGITAL_RESET_N	Digital signal reset
12	GND	Signal ground
13	I2C_0_SCL	I2C bus 0
15	I2C_0_SDA	
14	I2C_1_SCL	I2C bus 1
16	I2C_1_SDA	

Table 3-4: Extension board µC interface

SV4	APIX I2S audio interface	
Pin	**Signal**	**Description**
2,4,6,8	GND	Signal ground
1	AX_I2S_FRCK	APIX2 digital audio interface. Monitor only! To asses APIX2 audio interface through this port remove resistors R233 - R240.
3	AX_I2S_BCK	
5	AX_I2S_DATA	
7	AX_MCLK	

Table 3-5: APIX I2S audio interface

SV5	POF interlace to µC UART	
Pin	**Signal**	**Description**
1	UC_UART_RX	UART interface
2	UC_UART_TX	
3	GND	Signal ground
4	DIG_VCC33	3.3V Supply for POF module

Table 3-6: POF interlace to µC UART

X1	Power supply input for board LDOs	
Pin	**Signal**	**Description**
1	DCDC_2V1	2.1 V Supply input (optional, if 12V DC/DC is disabled)
2	DCDC_3V9	3.9 V Supply input (optional, if 12V DC/DC is disabled)
3	GND	Signal ground
4	GND	Signal ground

Table 3-7: Power supply input for board LDOs

X2	APIX pixel interface to extension board	
Pin	**Signal**	**Description**
1,2,5,6,11,16	GND	Signal ground
3	AX_PX20	APIX2 Pixel interface
4	AX_PX19	
7	AX_PX18	
8	AX_PX17	
9	AX_PX16	
10	AX_PX15	
12	AX_PX4	
13	AX_PX3	
14	AX_PX2	
15	AX_PX1	

Table 3-8: APIX pixel interface1 to extension board

X3	APIX pixel interface to extension board	
Pin	**Signal**	**Description**
1,4,7,13,16	GND	Signal ground
2	AX_PX6	APIX2 Pixel interface
3	AX_PX5	
5	AX_PX11	
6	AX_PX12	
8	AX_PX9	
9	AX_PX10	
11	AX_PX13	
12	AX_PX14	
14	AX_PX7	
15	AX_PX8	

Table 3-9: APIX pixel interface2 to extension board

X4	APIX pixel interface to extension board	
Pin	**Signal**	**Description**
1,4,7,13,16	GND	Signal ground
2	AX_PX21	APIX2 Pixel interface
3	AX_PX22	
5	AX_PX28	
6	AX_PX27	
8	AX_PX26	
9	AX_PX25	
11	AX_PX30	
12	AX_PX29	
14	AX_PX24	
15	AX_PX23	

Table 3-10: APIX pixel interface3 to extension board

X5	APIX data interface to extension board
Pin	**Signal**
1,7,10,16	GND
2	AX_SPIS_CS2
3	AX_SPISS_RW__MII_TXD2
4	AX_SPIS_MB0__MII_RXD2__SBUP_D0
5	AX_SPIS_MB1__MII_RXDV__SBUP_D1
6	AX_MII_TXD3
8	AX_I2C_SD
9	AX_I2C_SCL
11-14	NC
15	AX_STATUS

Table 3-11: APIX data interface1 to extension board

X6	APIX data interface to extension board
Pin	**Signal**
1,6,11,16	GND
2	AX_SPIM_SDO__MII_CLK
3	AX_SPIM_SDI__MII_TXEN
4	AX_SPIM_SCK__MII_RXD1
5	AX_SPIM_CS0#__MII_RXD0
7	AX_SPIM_CS1#__MII_RXD3
8	AX_SPIM_CS2#
9	AX_SPIS_SDO
10	AX_SPIS_SDI
12	AX_SPIS_SCK
13	AX_SPIS_STALL__MII_COL
14	AX_SPIS_CS0#__MII_TXD0__SBDW_D0
14	AX_SPIS_CS1#__MII_TXD1__SBDW_D1

Table 3-12: APIX data interface2 to extension board

X10	Stereo audio line in
Pin	**Signal**
1	AD_ADC_RN_2
2	AD_ADC_RP_2
3	AD_ADC_LN_2
4	AD_ADC_LP_2
5	AD_ADC_RN_1
6	AD_ADC_RP_1
7	AD_ADC_LN_1
8	AD_ADC_LP_1

Table 3-13: APIX data interface2 to extension board

X10	Stereo audio line in
Pin	**Signal**
13	AX_SPIS_STALL__MII_COL
14	AX_SPIS_CS0#__MII_TXD0__SBDW_D0
14	AX_SPIS_CS1#__MII_TXD1__SBDW_D1

Table 3-13: APIX data interface2 to extension board

3.1.7 DIP Switches and buttons

S1	Power Supply Control	
Switch	**Status**	**Description**
1	ON	Shutdown 3.9V supply from DC/DC
2	ON	Shutdown 2.1V supply from DC/DC
3	ON	Shutdown power over APIX supply
4	ON	Enable power sequencing on DC/DC converter 2.1V before 3.9V

Table 3-14: Power Supply Control

S2	APIX2 Bootstrap		
Switch	**Status**	**Signal**	**Bootstrap**
1	ON=1, OFF=0	SPIS_MB0__MII_RXD2__SBUP_D0	Bst1
2	ON=1, OFF=0	SPIM_SCK__MII_RXD1	Bst2
3	ON=1, OFF=0	SPIS_SDO	Bst3
4	ON=1, OFF=0	SPIS_STALL__MII_COL	Bst4
5	ON=1, OFF=0	SPIM_SDO__MII_CLK	Bst5
6	ON=1, OFF=0	SPIS_MB1__MII_RXDV__SBUP_D1	Bst6
7	ON=1, OFF=0	not used	
8	ON	Tx / Rx Select for µC (ON = Tx; OFF = Rx)	

Table 3-15: APIX2 Bootstrap

* see user manual of APIX2 Tx for bootstrapping details of APIX2.

S4	µC dip switch for software configuration	
Switch	**Signal**	**Description**
1	UC_DIP_0	ON = Tri-State µC ports connected to APIX SPI slave and GPIOs OFF = APIX SPI slave and GPIOs driven from µC (default)
2	UC_DIP_1	ON=1, OFF=0
3	UC_DIP_2	ON=1, OFF=0
4	UC_DIP_3	ON=1, OFF=0

Table 3-16: µC software configuration

S6	µC EEPROM Configuration	
Switch	**Status**	**Signal**
1	ON=1, OFF=0	EEPROM Address - AD0
2	ON=1, OFF=0	EEPROM Address - AD1
3	ON=1, OFF=0	EEPROM Address - AD2
4	ON=1, OFF=0	EEPROM Write Protect

Table 3-17: µC software configuration

	Push Buttons	
Button	**Status**	**Description**
S3	ON	µC and Board Hardware Reset
S5	ON=1, OFF=0	Software Trigger

Table 3-18: Push Buttons

3.1.8 Jumpers

JP4	Set µC ISP mode	
Pins	**Status**	**Description**
1 - 2	closed	Set ISP mode after hardware reset
1 - 2	open	Disable ISP mode after hardware reset (default)

Table 3-19: µC ISP Mode

JP8	APIX2 Reset generation	
Pins	**Status**	**Description**
1 - 2	closed	APIX2 reset triggered from µC (default)
2 - 3	closed	APIX2 reset active
1,2,3	open	APIX2 reset (always) inactive

Table 3-20: APIX2 reset generation

SJ1, SJ2	Power down LVDS1, Power down LVDS2	
Pins	**Status**	**Description**
1 - 2	closed	Power down LVDS1 or LVDS2 converter
1 - 2	open	Disable Power down LVDS1 or LVDS2 converter (default)

Table 3-21: µC ISP Mode

4.0 Hardware Configurations

4.1 Power supply

4.1.1 12V Main Board supply

Normally the board is powered from a 12V DC voltage source. A DC/DC switcher generates 3.9V and 2.1V as input to the different LDOs providing 3.3V and 1.8V.

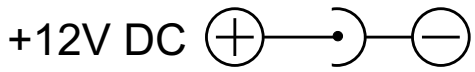


Figure 4-1: 12 V Main Power Plug (RAPC722)

4.1.2 Low noise board supply

To support EMI measurements the DC/DC switchers, mentioned above, can be disabled by the dip switch S1.1 and S1.2. The LDO input voltages can be supplied directly through X1.

4.1.3 Power over APIX (PoA)

The AC-coupling of the serial APIX IOs opens the possibility to transmit power over the APIX serial data lines. For details and consideration of PoA please see the application note AN202. The TX board provides a dedicated 18V / 2A extreme low noise power supply to demonstrate this feature and allows to remotely power up the RX application board.

4.2 Reset

After power up the board and especially the µC requires a hardware reset for proper function. The hardware reset is applied by pressing S3.

After hardware reset on S3 the µC generates a board reset signal (*DIGITAL_RESET_N*) for all board components, excluding APIX2. By placing a 0 ohm resistor on R189 and removing R190 the board reset (*DIGITAL_RESET_N*) can be coupled directly to the hardware reset generated from S3. (Bypassing the µC board reset generation)

Further, after hardware reset on S3 the µC generates a reset signal (*APIX_RESET_N*) for APIX2, if JP8.1 is connected with JP8.2. A manual APIX2 hardware reset can be generated when JP8.2 is pulled low, f.e. connecting JP8.2 with JP8.3.

ATTENTION: As APIX2 needs to be configured after reset, a manual reset on JP8.2 brings APIX2 in default mode, according the bootstrap settings. The µC does not handle the configuration of APIX2 in this case. To avoid any collision on the interface between µC and APIX2, S4.1 is required to be ON! Otherwise the board can be damaged!

4.3 LED Indicators

LED	LED Indicator	
Name	**Color**	**Description**
LED1	red	DC/DC switcher voltage 3.9V is on
LED2	red	DC/DC switcher voltage 2.1V is on
LED3	red	APIX2 reset is active
LED4	red	APIX2 status signal is high
LED5	red	µC hardware reset is active
LED6	red	Board hardware reset is active
LED7	green	µC USB LED
LED8	blue	µC alive (blink 1 sec)
LED9	red	tbd
LED10	yellow	tbd
LED11	yellow	µC suspend mode is active (All APIX interface signals high impedance)
LED12	yellow	USB Tx LED
LED13	red	USB Rx LED

Table 4-1: LED Indicators

5.0 Microcontroller - NXP LPC1768

5.1 Port description

Microcontroller Port Usage				
Pin	**µC Port**	**Signal**	**Direction**	**Description**
49	P0_11	AX_I2C_SCL	OC	APIX I2C master interface
48	P0_10	AX_I2C_SD	OC	
67	P2_6	AX_MII_TXD3	O_0	APIX2 Data Interface
66	P2_7	AX_SPIM_CS0#__MII_RXD0	I	
64	P2_9	AX_SPIM_CS1#__MII_RXD3	I	
63	P0_16	AX_SPIM_CS2#	I	
62	P0_15	AX_SPIM_SCK__MII_RXD1	I	
61	P0_17	AX_SPIM_SDI__MII_TXEN	I	
60	P0_18	AX_SPIM_SDO__MII_CLK	I	
81	P0_4	AX_SPIS_CS0#__MII_TXD0__SBDW_D0	O_1	
74	P2_1	AX_SPIS_CS1#__MII_TXD1__SBDW_D1	O_1	
79	P0_6	AX_SPIS_CS2#	O_1	
65	P2_8	AX_SPIS_MB0__MII_RXD2__SBUP_D0	I	
75	P2_0	AX_SPIS_MB1__MII_RXDV__SBUP_D1	I	
78	P0_7	AX_SPIS_SCK	O_0	
76	P0_9	AX_SPIS_SDI	O_0	
77	P0_8	AX_SPIS_SDO	I	
68	P2_5	AX_SPIS_STALL__MII_COL	I	
80	P0_5	AX_SPISS_RW__MII_TXD2	O_0	
6	P0_26	AX_STATUS	I	APIX2 Status
7	P0_25	HDMI_INT	I	Interrupt from HDMI interface
24	P0_28	I2C_0_SCL	OC	I2C Bus 0
25	P0_27	I2C_0_SDA	OC	
* O_0: Output (‘0’ at/after HW reset); O_1: Output (‘1’ at/after HW reset); I: Input				

Table 5-1: Microcontroller Port Usage

Microcontroller Port Usage				
Pin	**µC Port**	**Signal**	**Direction**	**Description**
47	P0_1	I2C_1_SCL	OC	I2C Bus 1
46	P0_0	I2C_1_SDA	OC	
73	P2_2	LED8	O_0	µC Alive LED (Blink)
70	P2_3	LED9	O_0	tbd
45	P1_29	LED10	O_0	tbd
44	P1_28	LED11	O_0	µC Suspend Mode Active
92	P1_8	RMII_CRS	I	Reduced MI interface of µC
87	P1_16	RMII_MDC	I	
86	P1_17	RMII_MDIO	I	
88	P1_15	RMII_REF_CLK	O_0	
91	P1_9	RMII_RXD0	I	
90	P1_10	RMII_RXD1	I	
89	P1_14	RMII_RXER	I	
95	P1_0	RMII_TXD0	O_0	
94	P1_1	RMII_TXD1	O_0	
93	P1_4	RMII_TXEN	O_0	
57	P0_21	UC_DIP_0	I	Apix Data Interface Suspend Mode Enable
58	P0_20	UC_DIP_1	I	tbd
33	P1_19	UC_DIP_2	I	tbd
34	P1_20	UC_DIP_3	I	tbd
53	P2_10	ISP_SELECT	I	Enable ISP mode
99	P0_3	UC_ISP_UART_RX	I	ISP Interface
98	P0_2	UC_ISP_UART_TX	O_0	
* O_0: Output (‘0’ at/after HW reset); O_1: Output (‘1’ at/after HW reset); I: Input				

Table 5-1: Microcontroller Port Usage

Microcontroller Port Usage				
Pin	**µC Port**	**Signal**	**Direction**	**Description**
100	RTCK	UC_JTAG_RTCK	I	µC JTAG Port
5	TCK	UC_JTAG_TCK	I	
2	TDI	UC_JTAG_TDI	I	
1	TDO	UC_JTAG_TDO	I	
3	TMS	UC_JTAG_TMS	I	
4	TRST	UC_JTAG_TRST	I	
56	P0_22	UC_P0_22	I	µC Interface to extension board. Place all ports to input until extension board exploration process is done or if no extension board is found.
9	P0_23	UC_P0_23	I	
8	P0_24	UC_P0_24	I	
35	P1_21	UC_P1_21	I	
36	P1_22	UC_P1_22	I	
37	P1_23	UC_P1_23	I	
38	P1_24	UC_P1_24	I	
39	P1_25	UC_P1_25	I	
52	P2_11	UC_P2_11	I	
51	P2_12	UC_P2_12	I	
50	P2_13	UC_P2_13	I	
17	RESET	UC_RESET_N	I	Hardware Reset
69	P2_4	UC_RESET_REQUEST_N	O_1	Reset Output
14	RSTOUT	RESET_OUT_N	O	
59	P0_19	APIX_RESET_REQ_N	O_1	APIX HW Reset
85	P4_29	UC_UART_RX	I	PC Communication UART
82	P4_28	UC_UART_TX	O_0	
30	USB_D-	UC_USBDN		PC USB Interface (disabled)
29	USB_D+	UC_USBDP		
32	P1_18	USB_LED		
21	VBUS	USB_VBUS		
* O_0: Output (‘0’ at/after HW reset); O_1: Output (‘1’ at/after HW reset); I: Input				

Table 5-1: Microcontroller Port Usage

6.0 Extension Boards (optional)

The APIX2_ADK boards are designed to be easily extended with application specific boards. The following extender boards are available:

- APIX2_ADK_ETH: Ethernet Extender board. The board includes a 3 port Ethernet switch with a MII interface, which allows to directly forward Ethernet traffic over the APIX link
- APIX2_ADK_EXT: I/O Extender board. The board allows to route all INAP375T/R pins to a separate board with headers for each pin.

6.1 Ethernet Extender Board

6.1.1 Description

The Ethernet board contains a Micrel KSZ8893MQL 3-port Ethernet switch, which offers two integrated ethernet PHYs and 1 MII interface. The MII interface is routed through flex cables to the TX/RX main board. The controller is also completely powered and configured by the master board.

The two integrated PHYs are brought out to two RJ45 connectors. Each can be used to connect another ethernet device, whose traffic will be forwarded through the APIX link.

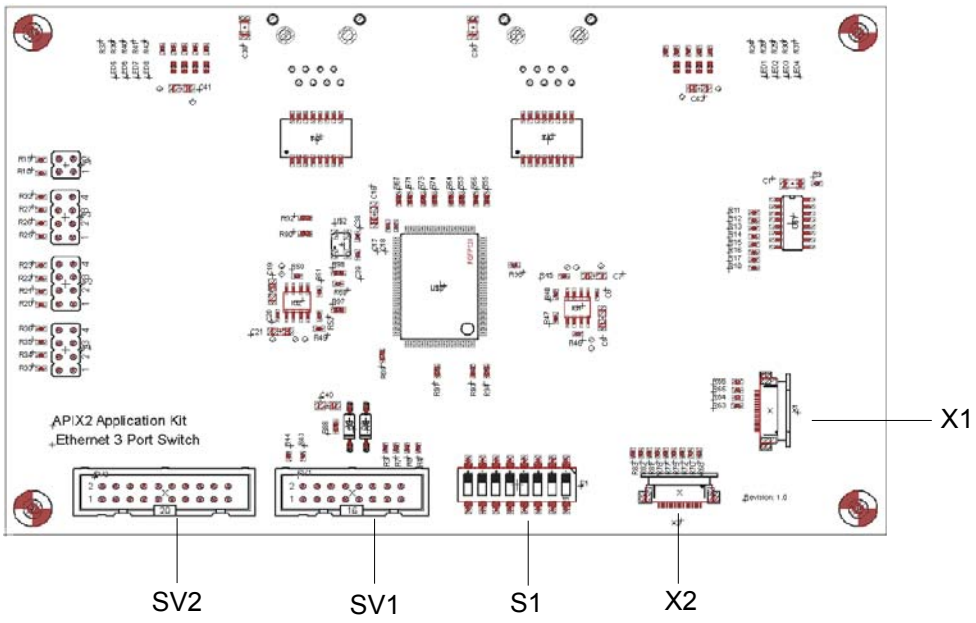


Figure 6-1: Ethernet board Top View

The connectors SV1, SV2, X1 and X2 need to be connected through specific cables provided with the kit to the master boards.

Master board connector	Ethernet board connector	Description
SV1	SV1	Power supply
SV2	SV2	Control signals
X5	X1	Data lines
X6	X2	Data lines

Table 6-2: Interconnect between Ethernet and Master board

Dip Switch S1 needs to be set to 00011000 ([8:1]).

6.1.2 Board Setup

The following steps illustrate how to hook together TX master board and the Ethernet board. With the Ethernet board Inova semiconductors ships one 20pin cable, one 16 pin cable and two 20pin (white flex cables). Also included are additional bolts acting as stand and distance bolts.

Start with connecting the grey power and control cables as well as the flex cables to the Ethernet board.The white flex cables need to be mounted with the connecting side up.

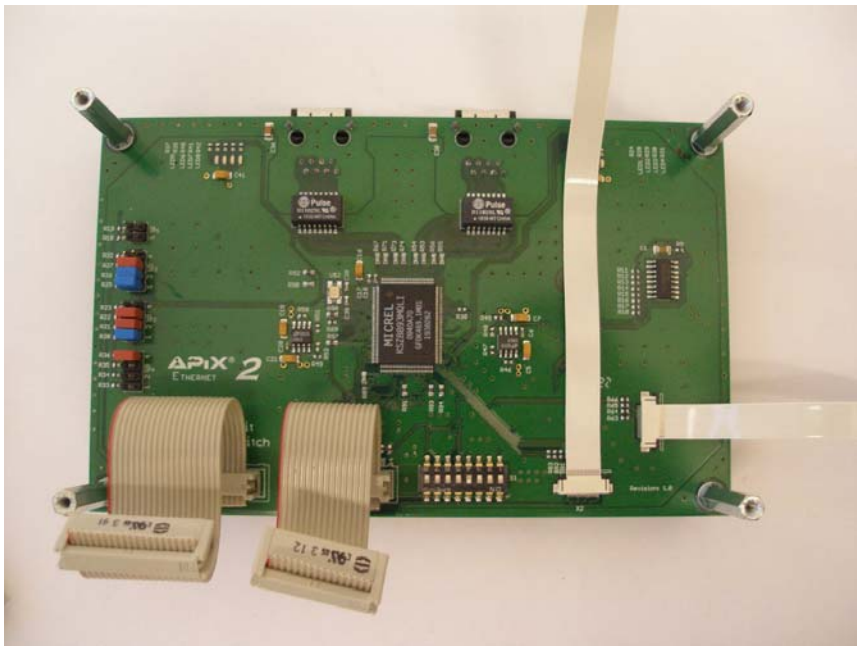


Figure 6-2: Cable connections to the Ethernet board

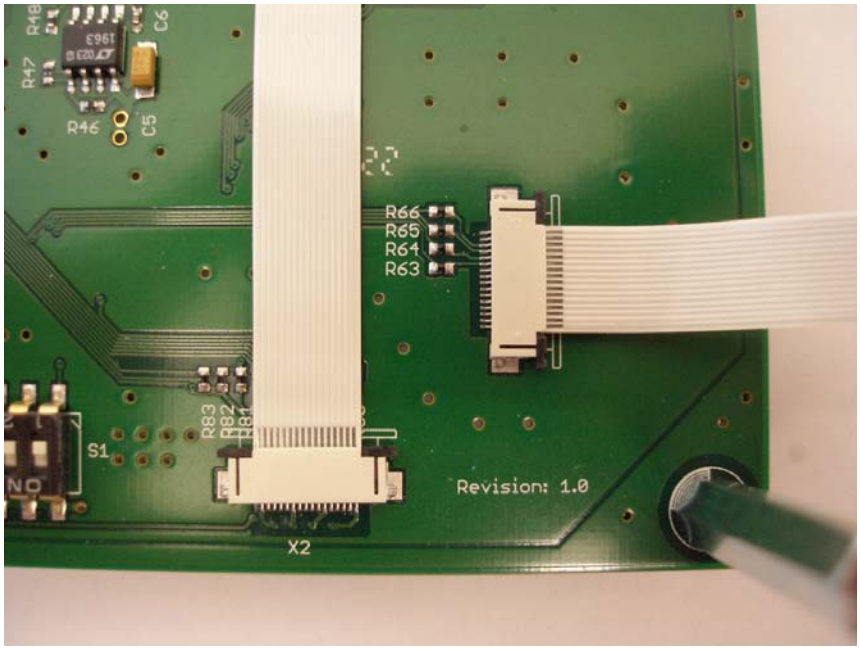


Figure 6-3: Flex cables with connecting side up

Afterwards, connect the white flex cables to the main board.

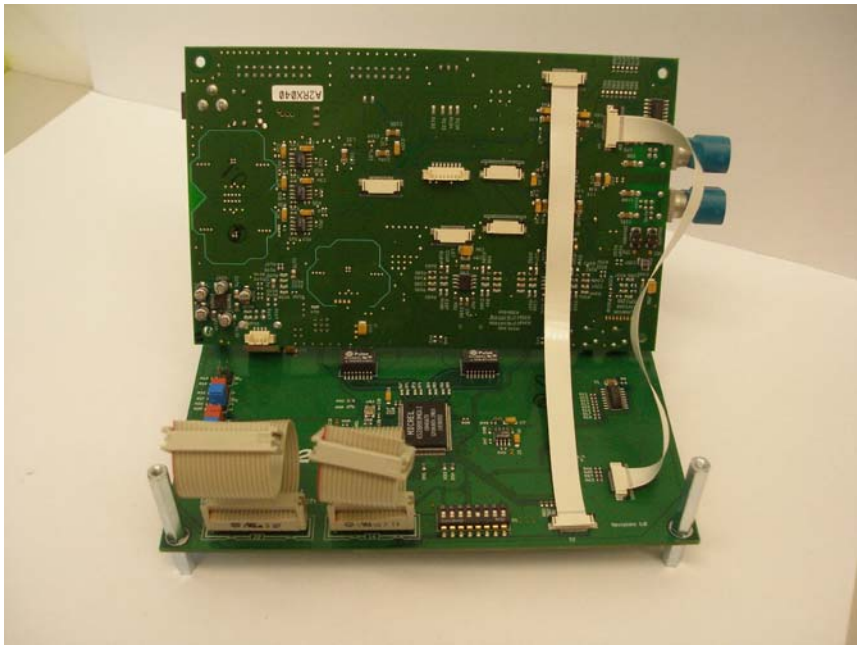


Figure 6-4: Connect white data cables to main board

Finally place the main board on top of the Ethernet board, connect the power supply and control connectors and fix it with the 4 screws. Please be careful to avoid bending the flex cables.

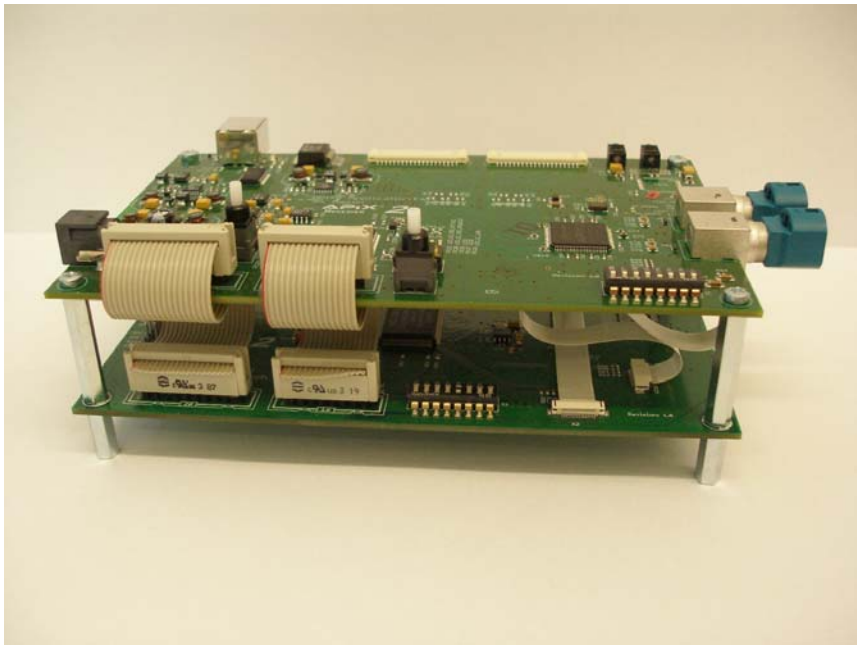


Figure 6-5: Complete APIX2_ADK with Ethernet board

6.2 I/O Extender board

6.2.1 Description

The IO Extender provides access to all interface pins of the INAP375T. This allows to directly connect to the video (RGB/LVDS), SPI or MII interfaces of the device.

The IO Extender kit includes

- IO Extender board
- 20pin power cable (grey)
- 16pin control cabe (grey)
- 5x 20pin flex cable (white)
- 4x bolts 20mm
- 4x bolts 30mm

The bolts are used as stands but also as mechanical distance bolt to the main board.

6.2.2 Connector description

6.2.2.1 Top view

The top side of the board is used to interconnect with the TX main board.

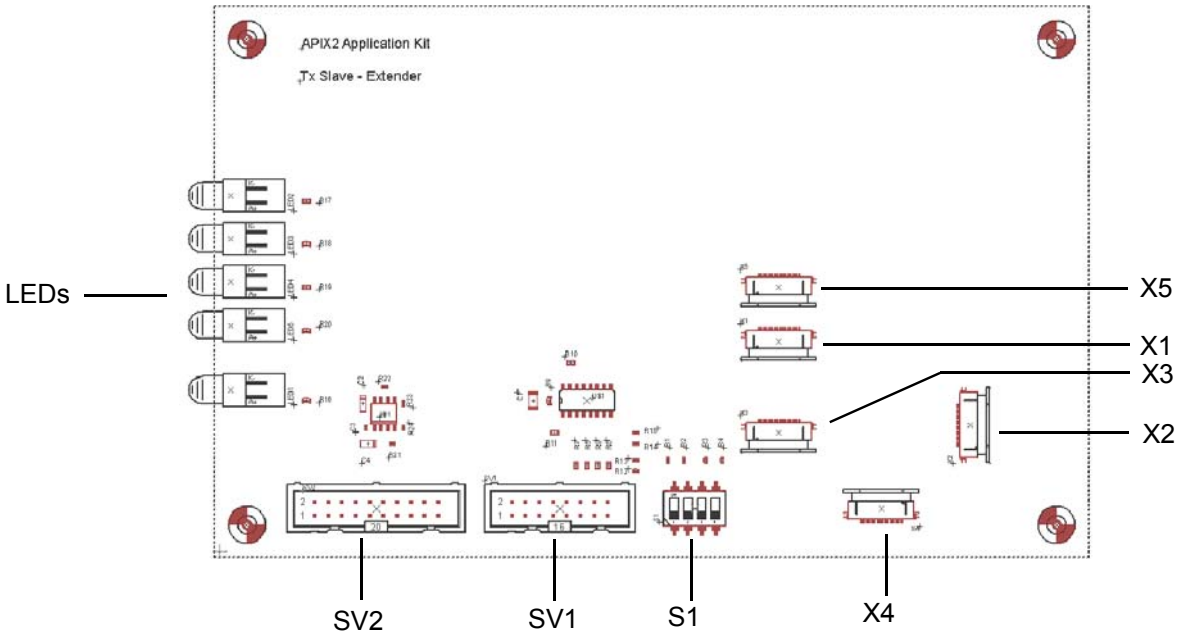


Figure 6-6: IO Extender Top view

Master board connector	IO Extender board connector	Description
SV1	SV1	Power supply
SV2	SV2	Control signals
X2	X1	Video interface

Table 6-3: Interconnection between Master and IO Extender

Master board connector	IO Extender board connector	Description
X3	X3	Video interface
X4	X5	Video Interface
X5	X2	Data interface (MII, SPI, I2C, I2S)
X6	X4	Data interface (SPI, MII)

Table 6-3: Interconnection between Master and IO Extender

The video interface of the IO Extender board should only be connected to the master in case an external video source shall be used.

IMPORTANT: In case X1, X3 and X5 of the IO Extender are connected to the TX master, the following resistors at the TX Master need to be removed:

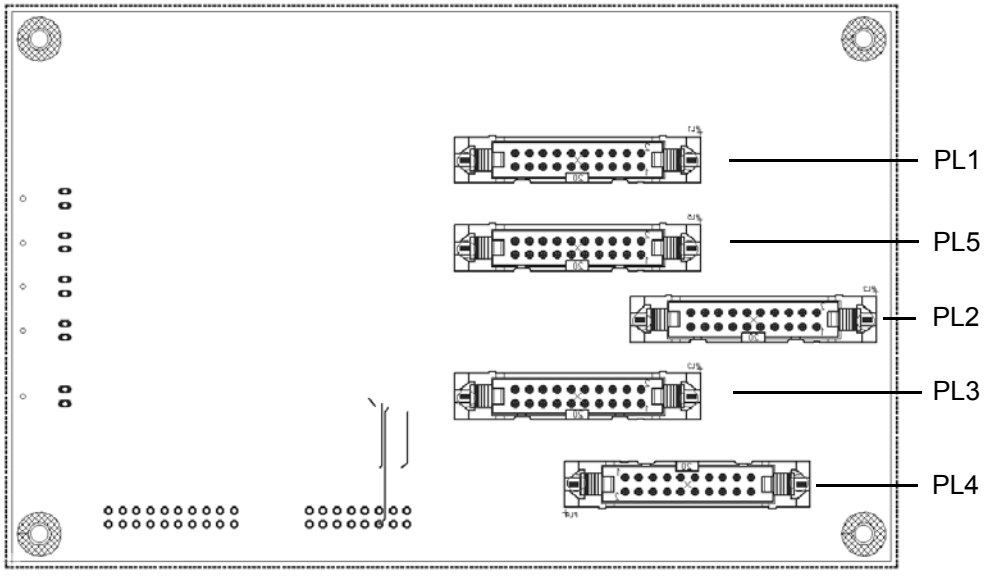
- Serial resistors: R49, R50, R52, R53, R55, R56, R58, R59, R61, R62, R64, R65, R67, R68, R71, R72, R75, R76, R78, R79
- In case of external RGB interface, termination resistors: R51, R54, R57, R60, R63, R66, R69, R73, R77, R80

In addition, the following resistors need to be removed to decouple the direct HDMI RGB pixel path (by default not mounted): R86, R88 .... R138, R140.

Dip Switch S1 needs be configured to 1100 ([4:1]) for correct operation.

6.2.2.2 Bottom view

All headers for the direct pin access are placed at the bottom of the board.



6.2.2.2.1 Pin Header PL1

Pin	Signal	Pin	Signal
1	PX20	11	PX15
2	GND	12	GND
3	PX19	13	PX4
4	GND	14	GND
5	PX18	15	PX3
6	GND	16	GND
7	PX17	17	PX2
8	GND	18	GND
9	PX16	19	PX1
10	GND	20	GND

Table 6-4: Pin Header PL1

6.2.2.2.2 Pin Header PL2

Pin	Signal	Pin	Signal
1	SPI_S_CS2#	11	I2S_DATA
2	GND	12	GND
3	SPI_S_RW/MII_TXD2	13	I2S_BCK
4	GND	14	GND
5	SPI_S_MB0/MII_RXD2/SBUP_DATA0	15	I2S_FRCK
6	GND	16	GND
7	MII_TXD3	17	I2S_MCLK
8	SPI_S_MB1/MII_RXDV/SBUP_DATA1	18	GND
9	I2C_SCL	19	STATUS
10	I2C_SD	20	GND

Table 6-5: Pin Header PL2

6.2.2.2.3 Pin Header PL3

Pin	Signal	Pin	Signal
1	GND	11	PX10
2	GND	12	PX9
3	PX5	13	GND
4	PX6	14	GND
5	GND	15	PX14
6	GND	16	PX13
7	PX12	17	GND
8	PX11	18	GND
9	GND	19	PX8
10	GND	20	PX7

Table 6-6: Pin Header PL3

6.2.2.2.4 Pin Header PL4

Pin	Signal	Pin	Signal
1	GND	11	SPI_S_SDO
2	SPI_M_SDO/MII_CLK	12	SPI_S_SDI
3	GND	13	GND
4	SPI_M_SDI/MII_TXEN	14	SPI_S_SCK
5	GND	15	GND
6	SPI_M_SCK/MII_RXD1	16	SPI_S_STALL/MII_COL
7	GND	17	GND
8	SPI_M_CS0#MII_RXD0	18	SPI_S_CS0#/MII_TXD0/SBDWN_DATA0
9	SPI_M_CS1#/MII_RXD3	19	GND
10	SPI_M_CS2#	20	SPI_S_CS1#/MII_TXD1/SBDWN_DATA1

Table 6-7: Pin Header PL4

6.2.2.2.5 Pin Header PL5

Pin	Signal	Pin	Signal
1	GND	11	PX25
2	GND	12	PX26
3	PX22	13	GND
4	PX21	14	GND
5	GND	15	PX29
6	GND	16	PX30
7	PX27	17	GND
8	PX28	18	GND
9	GND	19	PX23
10	GND	20	PX24

Table 6-8: Pin Header PL5

6.2.3 Board setup

The following steps illustrate how to hook together TX master board and the I/O Extender board.

Start with connecting the grey power and control cables as well as the flex cables to the Extender board.The white flex cables need to be mounted with the connecting side up. It is recommended to only connect those cables required to be routed to the pins. Please also refer to Section 6.2.1 in case the video interface is brought to the IO Extender board (X1, X3, X5)

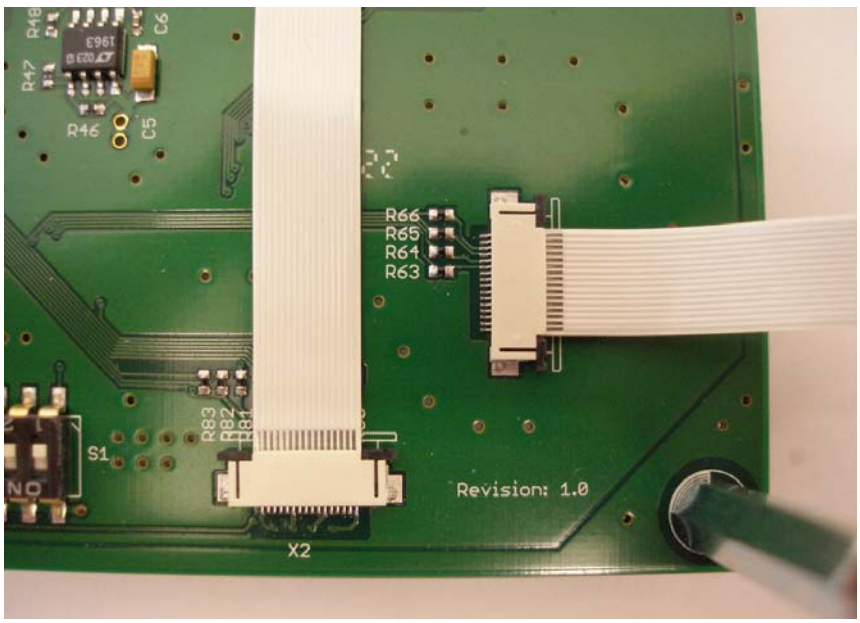


Figure 6-7: Flex cables with connecting side up

Afterwards, connect the white flex cables to the main board. Finally place the main board on top of the Ethernet board, connect the power supply and control connectors and fix it with the 4 screws. Please be careful to avoid bending the flex cables.

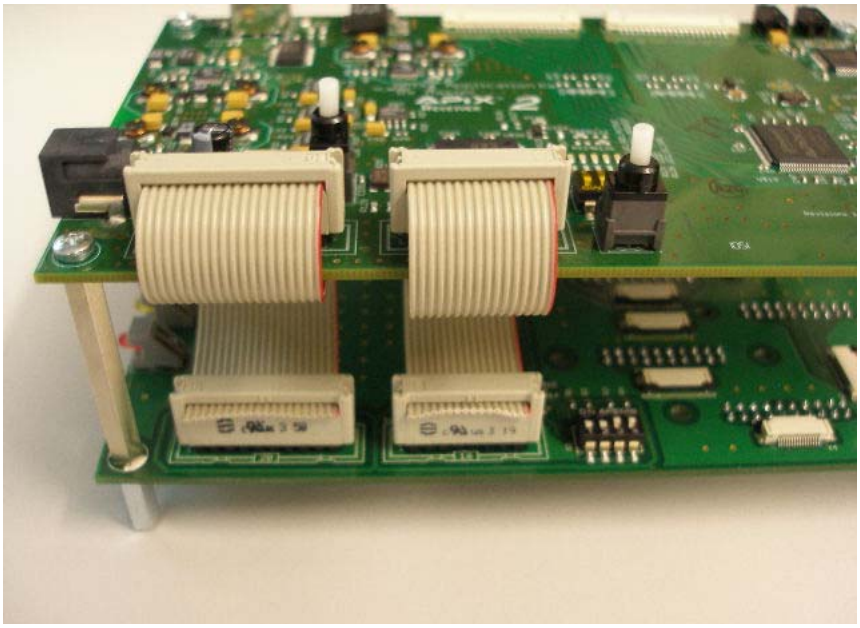


Figure 6-8: Complete APIX2_ADK with Ethernet board

7.0 Troubleshooting

7.1 Possible Issues

The following table assumes a transmitter and receiver device, correctly configured to transmit video over the ADK. Please refer to [1] - APICO User Manual, Inova Semiconductors GmbH or [3] - INAP375T/R Usermanual, Inova Semiconductors GmbH for further information regarding configuration.

Problem	Indicators	Possible solution
No picture	TX: st_px_ch0_timgen_locked=1 RX: st_px_ch0_synth_locked=1 st_px_ch0_timing_locked=1 st_px_ch0_clksyn_rdy=1	Link transmits a video but isn't displayed correctly Possible root cause: Wrong EDID The default EDID provided with APICO might not match the monitor in your setup. In case the picture doesn't come out, it might be necessary to read back the EDID for the monitor (connect the monitor to the PC and read back the EDID using an EDID tool) and use that EDID instead of the default EDID. Please check the APICO User manual how to change the EDID file for the HDMI inputs.
No picture	TX: st_px_ch0_timgen_locked=0 RX: st_px_ch0_synth_locked=0	INAP375T doesn't receive a correct image. Please check the video source, if it correctly detected the APIX2_ADK as monitor and if the resolution and video timing applied is within the limits of the INAP375T timing analyzer. Additionally reset the LVDS Transmitters as described in section 7.2

Table 7-9: Troubleshooting

7.2 Reset LVDS transmitters

After powering up the ADK board, or after changing the transmitter input clock of DS90C385, provide a 1 second pulse of 0 Volts at PWR DOWN pin by short circuiting the jumper SJ1/SJ2 (depending on application).

"The transmitter input clock must always be present when the device is enabled (PWR DOWN = HIGH). If the clock is stopped, the PWR DOWN pin must be used to disable the PLL. The PWR DOWN pin must be held low until after the input clock signal has been reapplied. This will ensure a proper device reset and PLL lock to occur. The transmitter input clock may be applied prior to powering up and enabling the transmitter. The transmitter input clock may also be applied after power up; however, the use of the PWR DOWN pin is required as described in the Transmitter Input Clock section." **(see datasheet of DS90C385)**

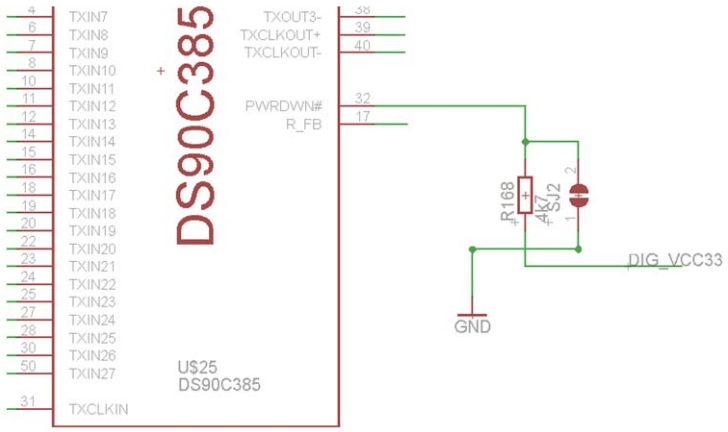


Figure 7-9: Schematic diagram for the connections to PWR DOWN pin on ADK INAP 375T

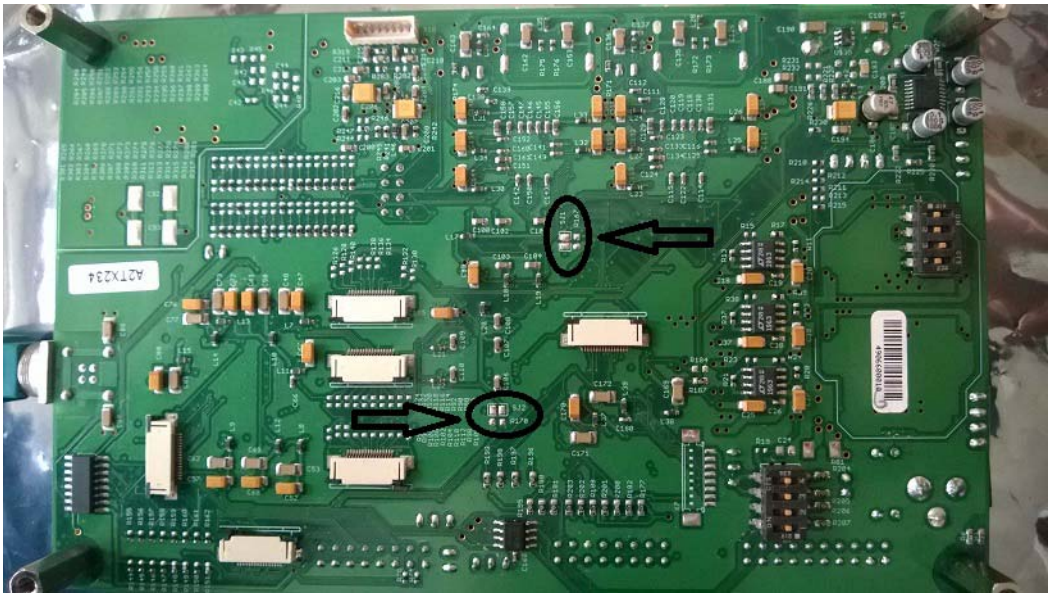


Figure 7-10: Locations of SJ1 and SJ2 jumper connections on the ADK board (bottom view)

8.0 Ordering information

The APIX2 ADK Transmitter board can be ordered via the order code below.

Ordering Code	Description
APIX2_ADK_TX	APIX2 ADK Transmitter Demonstration Board with HSD Connector
APIX2_ADK_TX_EXT	APIX2 ADK IO Extender Board
APIX2_ADK_ETH	APIX2 ADK Ethernet Extender Board

Table 10: Ordering Information

Kit contents :

- APIX2 ADK Transmitter Board
- 12V AC/DC supply
- USB Cable
- APIX2 ADK Demonstration Kit CD containing
  - APIX2 ADK Transmitter Hardware User Manual (this document)
  - APIX2 ADK Receiver Hardware User Manual
  - APIX2 ADK Software User Manual
  - INAP375T and INAP375R datasheet
  - Schematics
  - Gerberfiles

9.0 Revision History

Revision	Date	Changes
1.0	March 2012	Initial Release
1.1	May 2012	Corrected Table 6-2, “Interconnect between Ethernet and Master board,” on page 25 Corrected Table 6-3, “Interconnection between Master and IO Extender,” on page 28
1.2	March 2015	Added Section Section 7.0 "Troubleshooting" Corrected Table 6-1, “Ethernet board Top View,” on page 24, swapped X1 and X2 Corrected Table 6-2, “Interconnect between Ethernet and Master board,” on page 25

Table 11: Revision History

10.0 References

[1] – APICO User Manual, Inova Semiconductors GmbH

[2] – INAP375T/R Datasheets, Inova Semiconductors GmbH

[3] – INAP375T/R Usermanual, Inova Semiconductors GmbH

Inova Semiconductors GmbH
Grafinger Str. 26
D-81671 Munich / Germany
Phone: +49 (0)89 / 45 74 75 - 60
Fax: +49 (0)89 / 45 74 75 - 88
Email: info@inova-semiconductors.de
URL: http://www.inova-semiconductors.com