3GBit/s Digital Automotive Pixel Link Transmitter

INAP560T
INAP590T

The INAP560T is a high-speed digital multi-channel SerDes transmitter for infotainment applications. The highly scalable physical layer is APIX2 compatible and based on the APIX3 technology providing forward compatibility accordingly. It establishes a DC-balanced, AC coupled, low latency, point-to-point link over Star Quad (STQ) cables.

The INAP560T supports popular automotive displays with HD (High Definition) video resolutions up to 24 bit color depth. The device offers an HDMI 1.4 compliant video interface. Leveraging the HDMI 3D functionality, the device is able to receive and distinguish 2 independent video streams for transmission over the APIX2 link in point-to-point or daisy-chain applications.

The product version INAP590T supports High-bandwidth Digital Content Protection according to HDCP 1.4. It incorporates the encryption mechanisms as well as the required keys to transmit two independent streams of HDCP 1.4 encoded video and audio content over the APIX2 link.

In addition to the video transmission, the INAP560T provides independent full-duplex data communication channels. Using Inova's proprietary AShell protocol, secure data transfers are provided by error detection and automatic retransmission mechanisms. With its Media Independent Interfaces (MII/RMII), the INAP560T can directly connect to standard 100Mbit-Ethernet Media Access Controllers. Additionally, the link is optimized to carry low latency GPIO signals for reset or synchronization purposes. The built-in audio path allows synchronous TDM transmission of up to 8 audio channels, with accurate clock regeneration at the receiver for demanding infotainment applications. The high-speed serial driver can be pre-configured to adjust the characteristics of the physical layer to the transmission link and its specific PCB layout, cables and connectors.

Applications:

- Infotainment Systems
- Rear-Seat Entertainment Systems
- Cluster Applications

Features:

- Flexible physical layer supporting
  - 3 Gbps downstream (APIX2)
  - 187.5 Mbps upstream
  - up to 12 Gbps downstream for physical layer testing (PRBS)
- Supports 2 independent video streams
- HDMI 1.4a interface with 3D support
  - Support for RGB and YUV color coding
- 2 HDCP encryption engines (INAP590T only)
  - supports source encryption and repeater functionality
- Video resolutions up to
  - 1920x720x24Bit@60Hz
  - 1920x1080x24Bit@30Hz
- Configurable full-duplex communication channel for Data, Ethernet or GPIO
  - MII or RMII interface
  - SPI data interfaces
  - GPIOs for direct signalling
- Embedded AShell protocol
- I²S Audio interface
  - supports 16/24/32 Bit word length
  - supports 44.1 kHz / 48 / 96 kHz sampling
  - TDM support for up to 8 channels
- Diagnostic Features:
  - Self test
  - Embedded diagnostics

Package:

- 151 pin aQFN

Temperature/Quality:

- -40°C to +95°/105°C
- AEC-Q100

1.0 Block Diagram

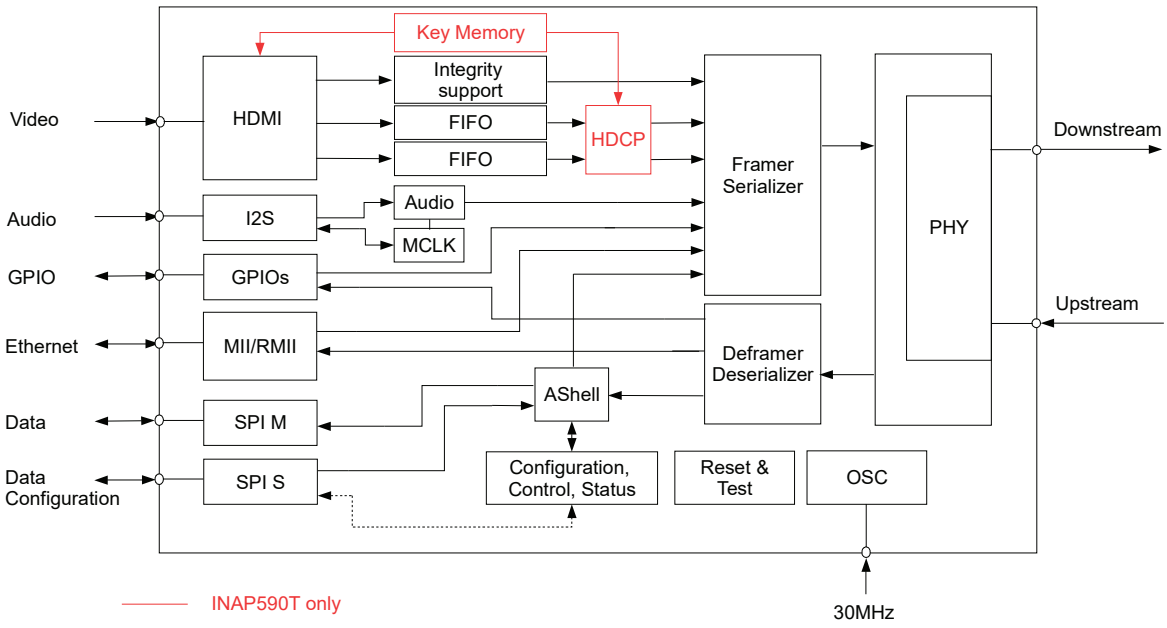

Figure 1-1: Block diagram

2.0 Physical Layer

The INAP560T/INAP590T physical layer is based on the third generation of APIX Technology - APIX3.

For test and qualification purposes, the physical layer of the INAP560T can be switched to APIX3 evaluation mode. In this mode, the device transmits test patterns of up to 6 Gbps at a single lane over Coax or shielded twisted pair (STP), as well as accumulated 12 Gbps (2x 6 Gbps) over STQ using the built in PRBS generator.

Even though the physical layer is based on APIX3 technology, the INAP560T/INAP590T only supports APIX2 functionality for video and data communication.

3.0 Electrical Characteristics

3.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{VDD}, V_{VDDA}	-0.5	1.32	V	
Digital IO Voltage	V_{VDDMII}, V_{VDD3}, V_{VDDH}	-0.5	3.63	V	
Analog IO Voltage	V_{VDDA3}, V_{VDDA_VCO},	-0.5	1.32	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Storage Temperature	T_{stg}	-55	+150	° C	
Max Soldering Temperature	T_{SLD} / T_{SLD}		260	° C	40 seconds maximum

Table 3-1: Absolute maximum ratings

3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Digital Core supply	V_{VDD}	1.14	1.2	1.26	V	
PHY Core supply	V_{VDDA}	1.14	1.2	1.26	V	
Digital IO Supply MII/RMII	V_{VDDMII}	1.71		3.46	V	Typical Operation at 1.8, 2.5 or 3.3V
Digital IO Supply	V_{VDD3}	1.71		3.46	V	Typical Operation at 1.8, 2.5 or 3.3V
Oscillator Supply	V_{VDDA_VCO}	1.14	1.2	1.26	V	
PHY IO supply	V_{VDDA3}	3.14	3.3	3.46	V	
HDMI IO supply	V_{VDDH}	3.14	3.3	3.46	V	
Ambient Temperature	T_a	-40	-	+105	° C	

Table 3-2: Recommended operating conditions

3.3 Supply currents

Parameter	Symbol	Min.	Typ. [a]	Max.	Units	Note
Digital Core supply	I_{VDD}		83	115	mA	
PHY Core supply	I_{VDDA}		80	100	mA	
Digital IO Supply [b]	I_{VDD3} + I_{VDDMII}		8	50	mA	
Digital IO Supply HDMI	I_{VDDH}		105	130	mA	
Oscillator Supply	I_{VDDA_VCO}		5	7	mA	
PHY IO supply (Single PHY)	V_{VDDA3}		27	105	mA	

Table 3-3: Supply currents

a. Typical values for APIX2 mode at 3GBit/s, MII at 25Mhz and a Pixel clock of 95MHz, HDCP disabled, 5m cable

b. IO Currents configured to minimum drive current. Maximum for MII interface and SPI slave interface active simultaneously

3.3.1 Supply current vs cable length

The following values reflect the typical power consumption values based on a Leoni Dacar 636 cable and the INAP560T evaluation board. Values in the final application may be different depending on the hardware layout and the selected cable.

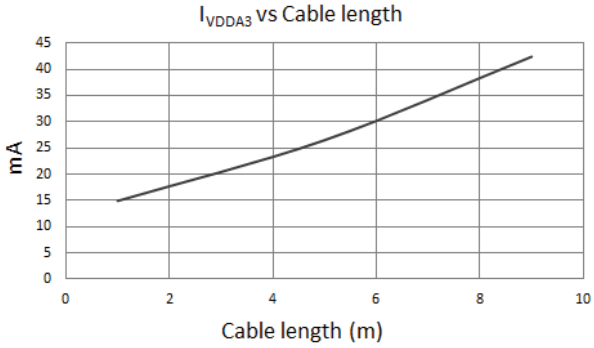

Figure 3-1: Supply current vs cable length

3.3.2 Supply current vs pixel clock frequency

The following values reflect the typical power consumption values for video transmission at 24-bit color depth.

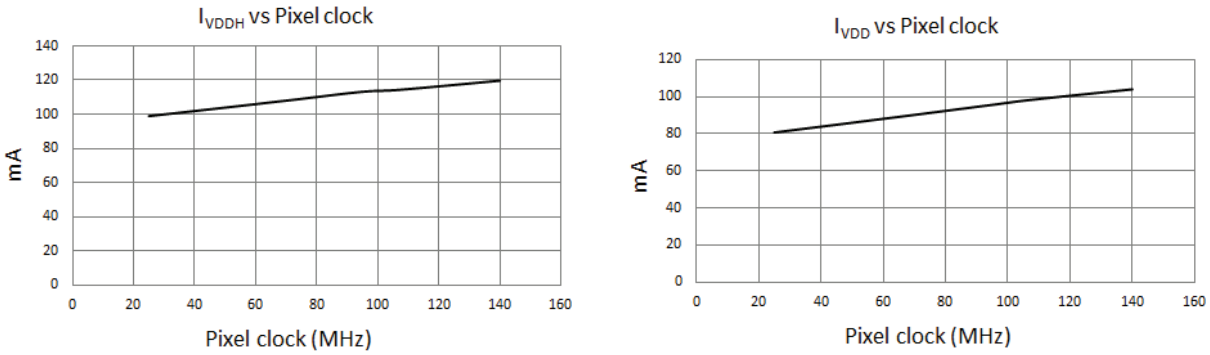

Figure 3-2: Supply current vs pixel clock frequency

3.4 Interface Characteristics

3.4.1 Serial Interface

The INAP560T downstream serial interface offers a flexible serial interface, with configurable pre-emphasis and digital filter structure. Data dependent deterministic jitter components, mainly introduced by ISI due to cable attenuation, can be compensated by pre-emphasis and equalization. Therefore only periodic and random jitter components are considered. The following values are determined for 3 Gbps mode.

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Periodic Jitter	$JP_{\delta-\delta}$	-	30	-	mUI	using 0101 pattern; parameter depends on application board, measured on characterization test board
Random Jitter	JR_{rms}	-	2.3	-	ps	using PRBS12 signal

Table 3-4: Downstream interface characteristics (TXDN0_P, TXDN0_N)

Parameter	Symbol	Min.	Max.	Units	Note
Differential input voltage range	V_{diff_in}	± 60	± 500	mV	
Serial input common mode range	V_{cmm_SDIN}	GND +0.7V + (V_{diff_in}/2)	V_{AVDD} +0.5V - (V_{diff_in}/2)	V	

Table 3-5: Upstream interface characteristics (TXDN1_P, TXDN1_N)

3.4.2 HDMI Interface

Parameter	Description	Min.	Typ.	Max	Units
BR	Serial Bit Rate	250		2250	Mbps
DREXT	REXT Resistance Error (470 ohms)	-1	0	1	%
T_{SKEW}	D2-0 [19:1] Skew	0		1100	ps
I_{DDL}	Supply Current 1.2V		110	160	mA
V_{IDIFF}	Input Differential Voltage	150		1200	mV
V_{ICM}	Input Common Mode Voltage (V_{VDDH}=3.3V +/-5%)	V_{VDDH} - 0.4		V_{VDDH}	V
RT	Input Termination Resistance	45	50	55	Ohm

Table 3-6: HDMI Interface electrical characteristics

3.4.3 Digital IOs

3.4.3.1 General Characteristics

The following characteristics are valid for MII/RMII, SPI_M, SPI_S, STATUS and GPIO functionality. All values specified for T_A=25°C. Load capacitance of 5pF. Drive strength configured to 4mA. V_{DVDD} refers to V_{VDD3} or V_{VDDMII} respectively.

Parameter	Description	Min.	Typ.	Max	Units
V_{IL}	Input Low Voltage	V_{VSS} - 0.3		0.3 * V_{DVDD}	V
V_{IH}	Input High Voltage	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	V_{DVDD} - 0.4			V
I_{OH}	Output Drive Current High, V_{OH}=2.9V	7.4	10.4	14.3	mA
I_{OL}	Output Drive Current Low, V_{OL}=0.4V	8.3	11.0	16.1	mA
I_L	Input Leakage Current, Receive Mode			<1	µA
t_{RO}	Output Rise Time (Slew Rate Fast) V_{DVDD} = 1.8V V_{DVDD} = 3.3V	 0.6 0.4	 1.0 0.8	 1.7 1.2	ns
t_{FO}	Output Fall Time (Slew Rate Fast) V_{DVDD} = 1.8V V_{DVDD} = 3.3V	 0.6 0.6	 1 0.8	 1.6 1.2	ns

Table 3-7: General IO Characteristics

3.4.3.2 SPI Slave Interface timing

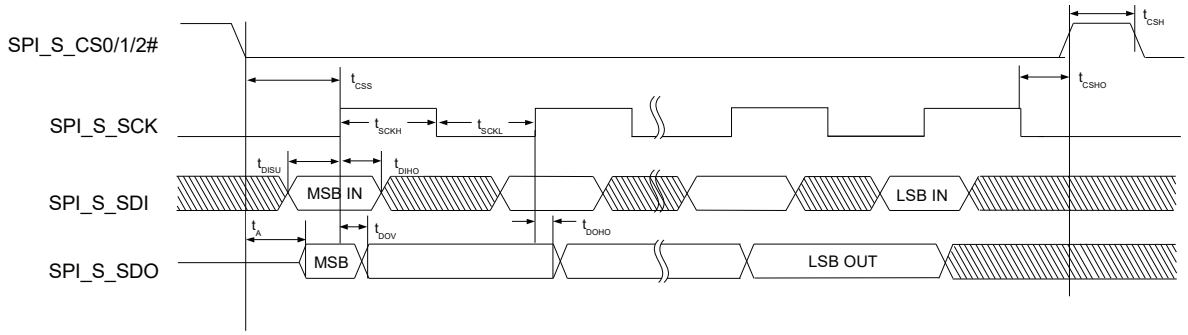

Figure 3-3: SPI Slave Timing Diagram

All values specified for T_A=25°C. $t_{SCK} = 1/f_{SCK}$.

Parameter	Description	Min	Max	Units
f_{SCK}	SCK Clock Frequency	-	30	MHz
t_{SCKH}	SCK High Time	6	-	ns
t_{SCKL}	SCK Low Time	6	-	ns
t_{CSH}	CS# High Time	22	-	ns
t_{CSS}	CS# Setup Time	64	-	ns
t_{CSHO}	CS# Hold Time	22	-	ns
t_{DISU}	Data In Setup Time	6	-	ns
t_{DIHO}	Data in Hold Time	6	-	ns
t_{DOV}	Data Output Valid	-	21	ns
t_{DOHO}	Data Output Hold Time	21	-	ns
t_A	Data Access Time	58	-	ns

Table 3-8: SPI Slave Interface characteristics

3.4.3.3 SPI Master Interface timing

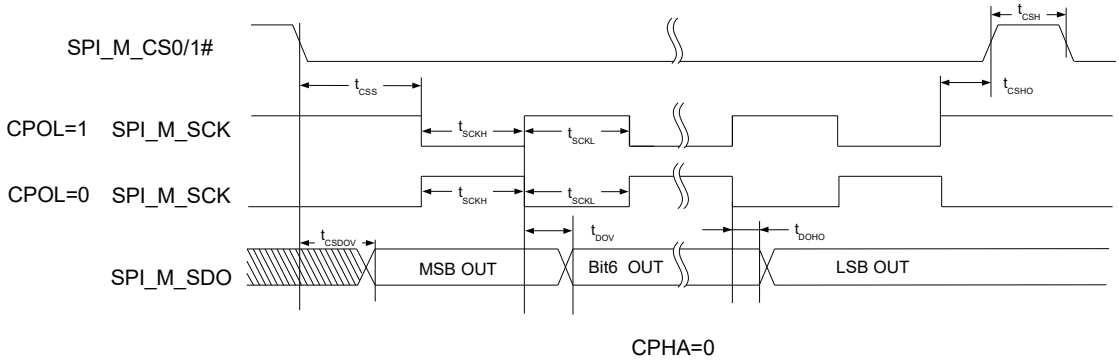

Figure 3-4: SPI Master Timing Diagram (CPHA=0)

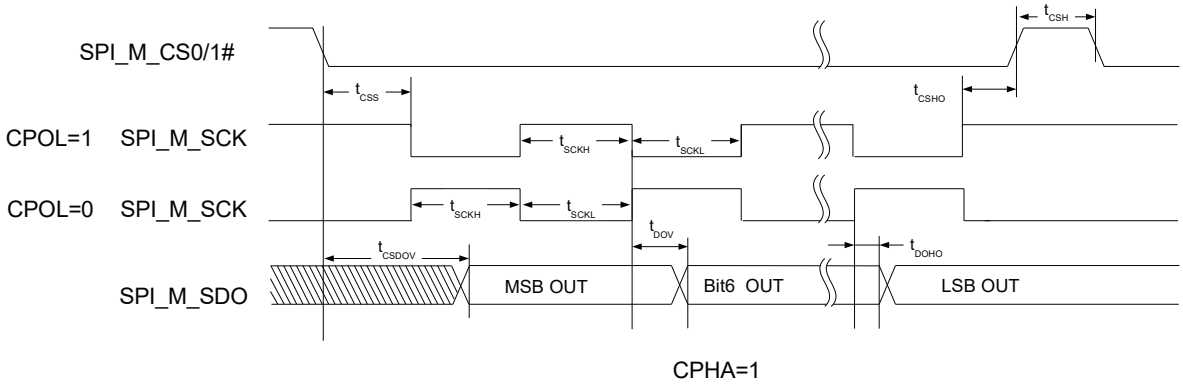

Figure 3-5: SPI Master Timing Diagram (CPHA=1)

Parameter	Description	Min.	Max.	Units
f_{SCK}[a]	SCK Clock Frequency	0.114	46.8	MHz
t_{SCKH}	SCK High Time	1/2 t_{fsck}	-	ns
t_{SCKL}	SCK Low Time	1/2 t_{fsck}	-	ns
t_{CSH}	CS# High Time	6	-	ns
t_{CSS}[b]	CS# Setup Time (configurable)	22	-	ns
t_{CSHO}[c]	CS# Hold Time	0	128	ns
t_{DOV}	Data Output Valid Time	-	1/2 t_{fsck}	ns
t_{DOHO}	Data Output Hold Time	1/2 t_{fsck}	-	ns
t_{CSDOV}	CS To Data Valid Time	-	1	ns

Table 3-9: SPI Master Interface characteristics

a. can be configured from core clock/16384 to core clock/8 by cfg_spi_m_clock_div
b. can be configured from 16 to 48 core clock cycles or multiples of t_{fsck} by cfg_spi_m_cs_delay
c. can be configured to no hold time or 24 core clock cycles

3.4.3.4 MII Interface Timings

$f_{MII\ CLK} = 1 / t_{PERIOD}$..

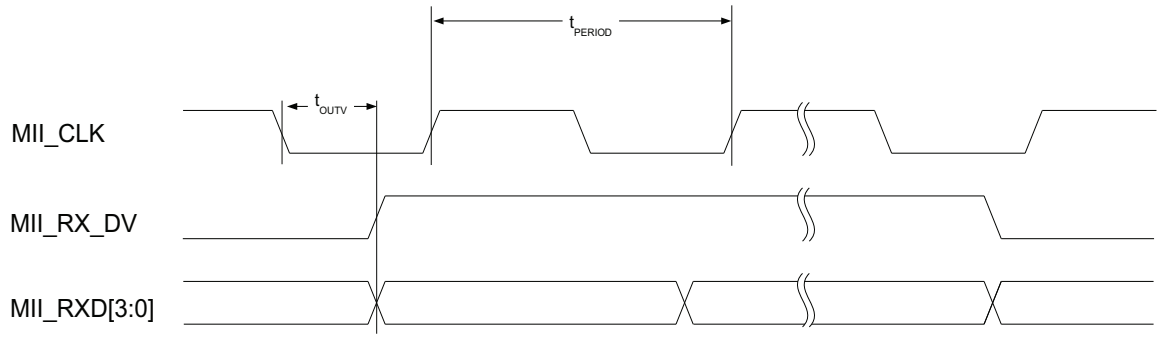

Figure 3-6: MII Interface Timing Diagram Transmit

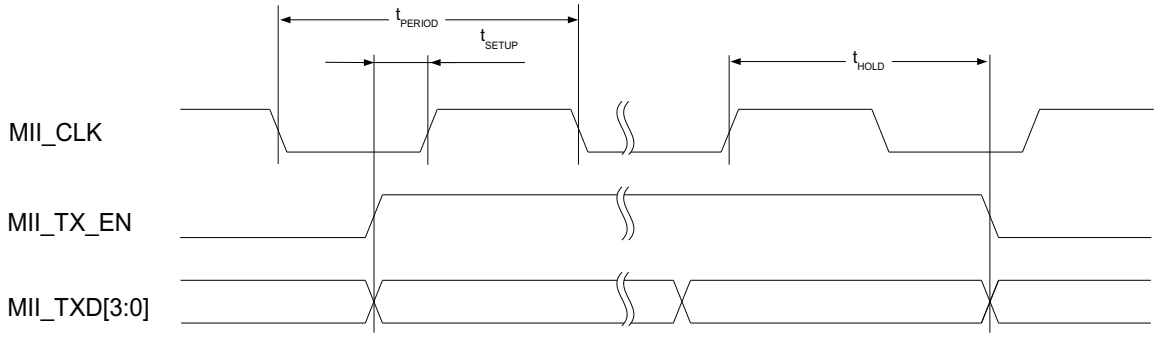

Figure 3-7: MII Interface Timing Diagram Receive

Parameter	Description	Min	Typ	Max	Units
f_{MII_CLK}	Clock Frequency	2.5	-	50	MHz
t_{SETUP}	Setup Time	9	-	-	ns
t_{HOLD}	Hold Time	0	-	-	ns
t_{OUTV}	Output Valid	1	-	7	ns

Table 3-10: MII Interface Timings

3.4.3.5 APFlag Interface

3.4.3.5.1 APFlag Interface Downstream

If configured as inputs, pins AP00_Flag and AP10_flag are sampled asynchronously and transmitted to configurable GPIO output ports at receiver side. The sampling frequency can be configured using parameters GPIO Bandwidth (gpio_bw_dwn) and GPIO halved (gpio_bw_div). For further information please refer to the INAP560T/INAP590T user manual. All values specified for T_A=25°C.

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Sampling Frequency.	Unit
3 GBit/s	1	high	off	26.768	MHz
3 GBit/s	1	low	off	6.696	MHz
3 GBit/s	1	high	on	13.393	MHz
3 GBit/s	1	low	on	3.348	MHz
3 GBit/s	2	high	off	13.393	MHz
3 GBit/s	2	low	off	3.348	MHz
3 GBit/s	2	high	on	6.696	MHz
3 GBit/s	2	low	on	unsupported	MHz

Table 3-11: GPIO Interface Downstream

3.4.3.5.2 APFlag interface upstream

Each of the pins AP00_FLAG, AP01_FLAG, AP10_FLAG and AP11_FLAG can be configured as APIX2 GPIO outputs, for which the data are coming from either one or two APIX2 receiver devices. The output frequency can be configured using parameter GPIO Bandwidth (gpio_bw_up). For further informations please refer to the INAP375T user manual. All values specified for T_A=25°C.

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
1	187.5 MBit/s	1	high	13.39	MHz
1	187.5 MBit/s	1	low	3.35	MHz
1	187.5 MBit/s	2	high	13.39	MHz
1	187.5 MBit/s	2	low	3.35	MHz
1	62.5 MBit/s	1	high	4.46	MHz
1	62.5 MBit/s	1	low	1.12	MHz
1	62.5 MBit/s	2	high	4.46	MHz
1	62.5 MBit/s	2	low	1.12	MHz
2	187.5 MBit/s	1	high	6.69	MHz

Table 3-12: GPIO Interface Upstream

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
2	187.5 MBit/s	1	low	3.35	MHz
2	187.5 MBit/s	2	high	6.96	MHz
2	187.5 MBit/s	2	low	3.35	MHz
2	62.5 MBit/s	1	high	2.23	MHz
2	62.5 MBit/s	1	low	1.12	MHz
2	62.5 MBit/s	2	high	2.23	MHz
2	62.5 MBit/s	2	low	1.12	MHz

Table 3-12: GPIO Interface Upstream

3.4.3.6 I²S Audio Interface

$f_{BCK} = 1 / t_{PERIOD}$. .

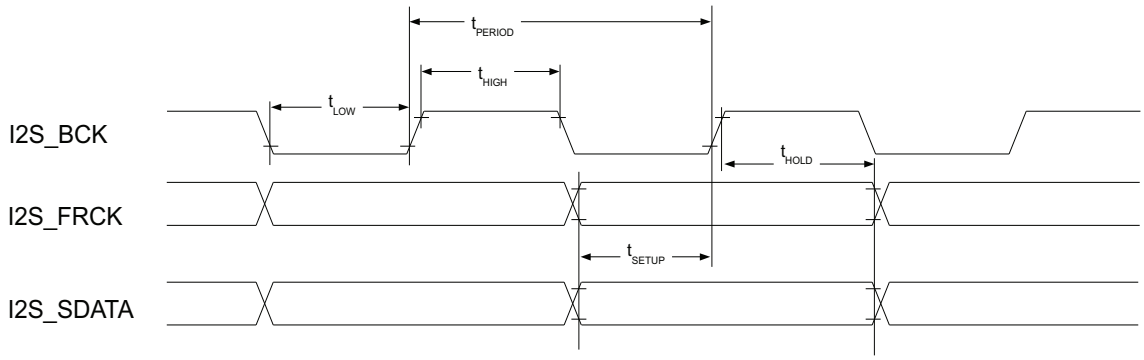

Figure 3-8: I2S Audio Interface Timing Diagram

Parameter	Description	Min	Max	Units
f_{BCK}	I2S_BCK frequency	0.75	26.78	MHz
t_{HIGH}	I2S_BCK high time	7	-	ns
t_{LOW}	I2S_BCK low time	7	-	ns
t_{SETUP}	Setup time	2	-	ns
t_{HOLD}	Hold time	7	-	ns

Table 3-13: I2S Audio Interface Timing

3.4.4 Reference Clock

The INAP560T requires an external clock source like a crystal or oscillator, acting as reference for the internal PLL.

Parameter	Symbol	min.	typ.	max.	Unit
Input voltage at XI[a]	V_{XI}	0		V_{VDD}	V
Nominal Frequency	f_{ref_osc}		30		MHZ
Frequency Tolerance	F_{TOL}	-100		+100	ppm

Table 3-14: Reference clock requirements

a. XI can be driven by an external clock for bypass operation. XO should never be driven or loaded by anything other than the oscillator crystal.

The internal oscillator has a fixed drive strength. In order to guarantee stable oscillation, the external crystal ESR and the capacitive loading on XI and XO should be selected to meet the conditions similar to the following table. The lower the ESR the higher the possible external load.

Equivalent Series Resistance (Ohm, ESR)	Capacitive Loading (pf, C)
20	<16
30	<12
40	<10
50	<8

Table 3-15: Typical ESR / Capacitive Load combinations

3.4.5 RESET and Boot strap timing

The INAP560T/INAP590T offers several boot strap pins to define, how the device will come up and check for a configuration after boot up or hardware reset. The correct boot strap selection is necessary for proper operation of the INAP560T/INAP590T device. See Section 4.1.1 for available boot strap options and pins.

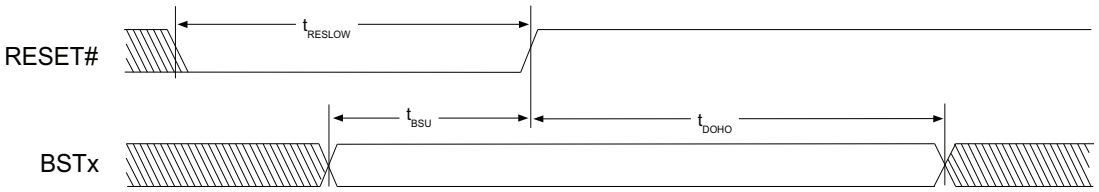

Figure 3-9: Reset and Boot Strap Timing Diagram

For a valid Reset Low Time (t_{RESLOW}) all supply voltages needs to be stable in the operating condition. At reset release (rising edge of RESET#) a stable reference clock is required. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
t_{RESLOW}	Reset Low Time	1	-	-	ms
t_{BSU}	Boot Strap In Setup Time	0	-	-	ns
t_{BHO}	Boot Strap in Hold Time	200	-	-	ns

Table 3-16: Boot Strap Reset Timing

4.0 Package Information

4.1 Pin description

4.1.1 Bootstrap options

The INAP560T offers several bootstrap options, which define the functionality of certain digital signal pins after hardware reset. The pin status is sampled after reset release.

Option	Boot strap pin					Description
	AP01_FLAG	AP11_FLAG	MB0	MB1	STATUS1	
BST_SPI_0					0	Dual SPI
BST_SPI_1					1	Single SPI
BST_MII_0	0			0		(reserved)
BST_MII_1	1			0		(reserved)
BST_MII_2	0			1		MII/RMII0 and IOs
BST_MII_3	1			1		(reserved)
BST_PHY_0			0			APIX3 Mode
BST_PHY_1			1			APIX2 Mode
BST_VDD_0		0				VDD3 = 1.8V
BST_VDD_1		1				VDD3 = 3.3V

Table 4-1: Boot-strap options

4.1.2 Pin list

The functionality of each pin is available in all BST_SPI and BST_MII bootstrap modes unless otherwise noted.

Pin Name	Pin	Type	Description
VDD	C2, F2, J3, M4, R4, R12, M12, M15, K12, J12, H12, G12, E13, E12, C13, B10, C5		Digital Core Power Supply 1.2 V
VDDMII	D2, G3, H1, L2		MII/RMII IO Power Supply (1.8V, 2.5V, 3.3V)
VDD3	N2, P3, R14, M14, B14, C11, D4		General IO Power Supply (1.8V, 2.5V, 3.3V)
VDDA	P5, P11, P8		PHY Core Power Supply 1.2V
VDDA_VCO	M8		Oscillator Power Supply 1.2V

Table 4-2: Pin list aQFN 151

Pin Name	Pin	Type	Description
VDDA3	R5, N7, N9, R11		PHY IO Power Supply 3.3V
VDDH	A10, D8, C6, D6, N5, P4		HDMI Power Supply 3.3V
VSS	R13, (exposed pad)		Ground
VSSH	D9, D7, A5		HDMI Ground
MII0_TXC	D3	I/O	BST_MII_2, BST_MII_3: MPIO_M13: Multipurpose IO (unused)
MII0_TX_CTL	E4	I/O	BST_MII_2, BST_MII_3: MII0_TX_EN: MII/RMII Interface 0 Transmit Enable Input
MII0_TXD0	C1	I/O	BST_MII_2, BST_MII_3: MII0_TXD0: MII/RMII Interface 0 Transmit Data Input 0
MII0_TXD1	E3	I/O	BST_MII_2, BST_MII_3: MII0_TXD1: MII/RMII Interface 0 Transmit Data Input 1
MII0_TXD2	F4	I/O	BST_MII_2, BST_MII_3: MII0_TXD2: MII Interface 0 Transmit Data Input 2
MII0_TXD3	D1	I/O	BST_MII_2, BST_MII_3: MII0_TXD3: MII Interface 0 Transmit Data Input 3
MII0_RXC	F3	I/O	BST_MII_2, BST_MII_3: MII0_CLK: MII/RMII Interface 0 Reference Clock Output
MII0_RX_CTL	E1	I/O	BST_MII_2, BST_MII_3: MII0_RX_DV: MII/RMII Interface 0 RX Data Valid Output
MII0_RXD0	G4	I/O	BST_MII_2, BST_MII_3: MII0_RXD0: MII/RMII Interface 0 Receive Data Output 0
MII0_RXD1	F1	I/O	BST_MII_2, BST_MII_3: MII0_RXD1: MII/RMII Interface 0 Receive Data Output 1
MII0_RXD2	G2	I/O	BST_MII_2, BST_MII_3: MII0_RXD2: MII Interface 0 Receive Data Output 2
MII0_RXD3	G1	I/O	BST_MII_2, BST_MII_3: MII0_RXD3: MII Interface 0 Receive Data Output 3
MII1_RXD3	H3	I/O	BST_MII_2: MPIO_M01: Multipurpose IO (unused) BST_MII_3: MII1_RXD3: MII Interface 1 Receive Data Output 3
MII1_RXD2	H2	I/O	BST_MII_2: MPIO_M02: Multipurpose IO (unused) BST_MII_3: MII1_RXD2: MII Interface 1 Receive Data Output 2

Table 4-2: Pin list aQFN 151

Pin Name	Pin	Type	Description
MII1_RXD1	J1	I/O	BST_MII_2: MPIO_M03: Multipurpose IO (unused) BST_MII_3: MII1_RXD1: MII/RMII Interface 1 Receive Data Output 1
MII1_RXD0	J2	I/O	BST_MII_2: MPIO_M04: Multipurpose IO (unused) BST_MII_3: MII1_RXD0: MII/RMII Interface 1 Receive Data Output 0
MII1_RX_CTL	J4	I/O	BST_MII_2: MPIO_M05: Multipurpose IO (unused) BST_MII_3: MII1_RX_DV: MII/RMII Interface 1 RX Data Valid output
MII1_RXC	K1	I/O	BST_MII_2: MPIO_M06: Multipurpose IO (unused) BST_MII_3: MII1_CLK: MII/RMII Interface 1 RX Reference Clock Output
MII1_TXD3	K3	I/O	BST_MII_2: MPIO_M07: Multipurpose IO (unused) BST_MII_3: MII1_TXD3: MII Interface 1 Transmit Data Input 3
MII1_TXD2	L1	I/O	BST_MII_2: MPIO_M08: Multipurpose IO (unused) BST_MII_3: MII1_TXD2: MII Interface 1 Transmit Data Input 2
MII1_TXD1	K4	I/O	BST_MII_2: MPIO_M09: Multipurpose IO (unused) BST_MII_3: MII1_TXD1: MII/RMII Interface 1 Transmit Data Input 1
MII1_TXD0	M1	I/O	BST_MII_2: MPIO_M10: Multipurpose IO (unused) BST_MII_3: MII1_TXD0: MII/RMII Interface 1 Transmit Data Input 0
MII1_TX_CTL	L3	I/O	BST_MII_2: MPIO_M11: Multipurpose IO (unused) BST_MII_3; MII1_TX_EN: MII/RMII Interface 1 Transmit Enable (TX_EN)
MII1_TXC	M2	I/O	BST_MII_2, BST_MII_3: MPIO_M12: Multipurpose IO (unused)
RESET_N	N1	I	Reset (Low Active)
TEST	L4	I	Test Mode Enable, pull down to GND (0 Ohm)

Table 4-2: Pin list aQFN 151

Pin Name	Pin	Type	Description
STATUS0	M3	O	Status Output 0
SPI_M_CS1_N	N3	I/O	BST_SPI_0: SPI Master Chip Select 1 Output (Low Active) BST_SPI_1: MPIO_10: Multipurpose IO (unused)
SPI_M_SCK	P2	I/O	BST_SPI_0: SPI Master Clock Output BST_SPI_1: MPIO_11: Multipurpose IO (unused)
SPI_M_SDO	M5	I/O	BST_SPI_0: SPI Master Data Output BST_SPI_1: MPIO_12: Multipurpose IO (unused)
SPI_M_CS0_N	N4	I/O	BST_SPI_0: SPI Master Chip Select 0 Output (Low Active) BST_SPI_1: SPI_S_RW: SPI Slave Read/Write request input
SPI_M_STALL[b]	P1	I	SPI Master Flow control pin
AP00_FLAG	R2	I/O	Application Flag 00
AP01_FLAG	R3	I/O	Application Flag 01 / Boot strap pin
TXDN1_P	M6	I/O	APIX Downstream Serial Output Channel 1
TXDN1_N	M7	I/O	APIX Downstream Serial Output Channel 1
ATST	N8	I/O	APIX Analog Test Port (leave open)
TXDN0_N	M9	I/O	APIX Downstream Serial Output Channel 0
TXDN0_P	M10	I/O	APIX Downstream Serial Output Channel 0
XI	N11	I	Oscillator Input (30MHz)
XO	P12	O	Oscillator Output (30MHz)
SPI_S_CS0_N[a]	P13	I	SPI Slave Chip Select 0 Input (Low Active)
SPI_S_CS1_N[a]	P14	I	SPI Slave Chip Select 1 Input (Low Active)
SPI_S_CS2_N[a]	N13	I	SPI Slave Chip Select 2 Input (Low Active)
AP11_FLAG	P15	I/O	Application Flag 11 / Boot strap pin
SPI_S_SCK	N14	I	SPI Slave Clock
SPI_S_SDI	M13	I	SPI Slave Data Input
SPI_S_SDO	N15	O	SPI Slave Data Output

Table 4-2: Pin list aQFN 151

Pin Name	Pin	Type	Description
SPI_S_STALL	L12	I	SPI Slave Flow Control
STATUS2	D12	O	Status Output 2
AP10_FLAG	B13	I/O	Application Flag 10
I2S_FRCK[b]	C12	I	I2S Frame clock Input
I2S_BCK[b]	D11	I	I2S Bit Clock Input
I2S_SDATA[b]	B12	I	I2S Data Input
I2S_MCLK	A12	I/O	I2S Master Clock In/Output
STATUS1	D10	I/O	Status Output 1 / Boot strap pin
DDC_SDA	A11	I/O	HDMI – I2C Data Line, Open-drain
DDC_SCL	C10	I/O	HDMI – I2C Clock Line, Open-drain
TMDSD2_P	B9	I	HDMI – TMDS Data line 2 P
TMDSD2_N	A9	I	HDMI – TMDS Data line 2 N
TMDSD1_P	B8	I	HDMI – TMDS Data line 1 P
TMDSD1_N	A8	I	HDMI – TMDS Data line 1 N
TMDSD0_P	A7	I	HDMI – TMDS Data line 0 P
TMDSD0_N	B7	I	HDMI – TMDS Data line 0 N
TMDSCK_P	A6	I	HDMI – TMDS Clock line P
TMDSCK_N	B6	I	HDMI – TMDS Clock line N
REXT	B5	O	HDMI – BIAS Resistor Output, connect with 4.7kOhm to GND
HDMI_MON	A4	O	HDMI – Monitor Output - leave open
MB0	B3	I/O	Mailbox 0 Output / Bootstrap pin

Table 4-2: Pin list aQFN 151

Pin Name	Pin	Type	Description
MB1	B2	I/O	Mailbox 1 Output / Bootstrap pin
ALIVE	C3	I/O	reserved
NC	A1,B1,A2, A3, A13, A14, A15, B15, B11, B4, D5, C4, L13, L14, L15, K13, K14, K15, J13, J14, H14, H13, G15, G14, G13, F15, F14, F13, E14, D15, C15, C14, R1, R15		do not connect, place pad for mechanical stability

Table 4-2: Pin list aQFN 151

a. Internal weak pull-up after reset
b. Internal weak pull-down after reset

4.2 Pin reset states

Pin Name	Pin	Type	Reset state
MII0_TXC	D3	I/O	Tri-State
MII0_TX_CTL	E4	I/O	Tri-State
MII0_TXD0	C1	I/O	Tri-State
MII0_TXD1	E3	I/O	Tri-State
MII0_TXD2	F4	I/O	Tri-State
MII0_TXD3	D1	I/O	Tri-State
MII0_RXC	F3	I/O	Tri-State
MII0_RX_CTL	E1	I/O	Tri-State
MII0_RXD0	G4	I/O	Tri-State
MII0_RXD1	F1	I/O	Tri-State
MII0_RXD2	G2	I/O	Tri-State
MII0_RXD3	G1	I/O	Tri-State
MII1_RXD3	H3	I/O	Tri-State
MII1_RXD2	H2	I/O	Tri-State
MII1_RXD1	J1	I/O	Tri-State
MII1_RXD0	J2	I/O	Tri-State
MII1_RX_CTL	J4	I/O	Tri-State
MII1_RXC	K1	I/O	Tri-State
MII1_TXD3	K3	I/O	Tri-State
MII1_TXD2	L1	I/O	Tri-State
MII1_TXD1	K4	I/O	Tri-State
MII1_TXD0	M1	I/O	Tri-State
MII1_TX_CTL	L3	I/O	Tri-State
MII1_TXC	M2	I/O	Tri-State
TEST	L4	I	Input
STATUS0	M3	I/O	Tri-State
SPI_M_CS1_N	N3	I/O	Tri-State
SPI_M_SCK	P2	I/O	Tri-State

Table 4-3: Reset state of all digital IO pins

Pin Name	Pin	Type	Reset state
SPI_M_SDO	M5	I/O	Tri-State
SPI_M_CS0_N	N4	I/O	Tri-State
SPI_M_STALL	P1	I/O	Tri-State
AP00_FLAG	R2	I/O	Tri-State
AP01_FLAG	R3	I/O	Tri-State
SPI_S_CS0_N	P13	I	Input, internal pull-up
SPI_S_CS1_N	P14	I	Input, internal pull-up
SPI_S_CS2_N	N13	I	Input, internal pull-up
AP11_FLAG	P15	I/O	Tri-State
SPI_S_SCK	N14	I	Input
SPI_S_SDI	M13	I	Input
SPI_S_SDO	N15	I	Input
SPI_S_STALL	L12	I	Input
STATUS2	D12	O	Tri-State
AP10_FLAG	B13	I/O	Tri-State
I2S_FRCK	C12	I	Input, internal pull-down
I2S_BCK	D11	I	Input, internal pull-down
I2S_SDATA	B12	I	Input, internal pull-down
I2S_MCLK	A12	I/O	Tri-State
STATUS1	D10	I/O	Tri-State
DDC_SDA	A11	I/O	Tri-State
DDC_SCL	C10	I/O	Tri-State
HDMI_MON	A4	O	Output
MB0	B3	I/O	Tri-State

Table 4-3: Reset state of all digital IO pins

Pin Name	Pin	Type	Reset state
MB1	B2	I/O	Tri-State
ALIVE	C3	I/O	Tri-State
NC	A1, A2, A3, A13, A15, A15, B1, B15, B11, B4, D5, C4, L13, L14, L15, K13, K14, K15, J13, J14, H14, H13, G15, G14, G13, F15, F14, F13, E14, D15, C15, C14, R1, R15		Tri-State

Table 4-3: Reset state of all digital IO pins

4.3 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	NC	HDMI_MON	VSSH	TMDSCK_P	TMDSD0_P	TMDSD1_N	TMDSD2_N	VDDH	DDC_SDA	I2S_MCLK	NC	NC	NC	A
B	NC	MB1	MB0	NC	REXT	TMDSCK_N	TMDSD0_N	TMDSD1_P	TMDSD2_P	VDD	NC	I2S_SDATA	AP10_FLAG	VDD3	NC	B
C	MII0_TXD0	VDD	ALIVE	NC	VDD	VDDH				DDC_SCL	VDD3	I2S_FRCK	VDD	NC	NC	C
D	MII0_TXD3	VDDMII	MII0_TXC	VDD3	NC	VDDH	VSSH	VDDH	VSSH	STATUS1	I2S_BCK	STATUS2			NC	D
E	MII0_RX_CTL		MII0_TXD1	MII0_TX_CTL								VDD	VDD	NC		E
F	MII0_RXD1	VDD	MII0_RXC	MII0_TXD2									NC	NC	NC	F
G	MII0_RXD3	MII0_RXD2	VDDMII	MII0_RXD0								VDD	NC	NC	NC	G
H	VDDMII	MII1_RXD2	MII1_RXD3									VDD	NC	NC		H
J	MII1_RXD1	MII1_RXD0	VDD	MII1_RX_CTL								VDD	NC	NC		J
K	MII1_RXC		MII1_TXD3	MII1_TXD1								VDD	NC	NC	NC	K
L	MII1_TXD2	VDDMII	MII1_TX_CTL	TEST								SPI_S_STALL	NC	NC	NC	L
M	MII1_TXD0	MII1_TXC	STATUS0	VDD	SPI_M_SDO	TXDN1_P	TXDN1_N	VDDA_VCO	TXDN0_N	TXDN0_P		VDD	SPI_S_SDI	VDD3	VDD	M
N	RESET_N	VDD3	SPI_M_CS1_N	SPI_M_CS0_N	VPP		VDDA3	ATST	VDDA3		XI		SPI_S_CS2_N	SPI_S_SCK	SPI_S_SDO	N
P	SPI_M_STALL	SPI_M_SCK	VDD3	VDDH	VDDA			VDDA			VDDA	XO	SPI_S_CS0_N	SPI_S_CS1_N	AP11_FLAG	P
R	NC	AP00_FLAG	AP00_FLAG	VDD	VDDA3						VDDA3	VDD	VSS	VDD3	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 4-1: Pinout Diagram

4.4 Package Dimensions

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.85
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2		0.675 REF	
L/F THICKNESS		A3		0.13 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.575	0.625	0.675
		b2		0.1 REF	
BODY SIZE	X	D		11 BSC	
	Y	E		11 BSC	
LEAD PITCH		e		0.7 BSC	
EP SIZE	X	J	4.2	4.3	4.4
	Y	K	4.2	4.3	4.4
LEAD LENGTH		L	0.575	0.625	0.675
		L1		0.1 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.2	
COPLANARITY		ccc		0.1	
LEAD OFFSET		ddd		0.08	
EXPOSED PAD TOLERANCE		eee		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

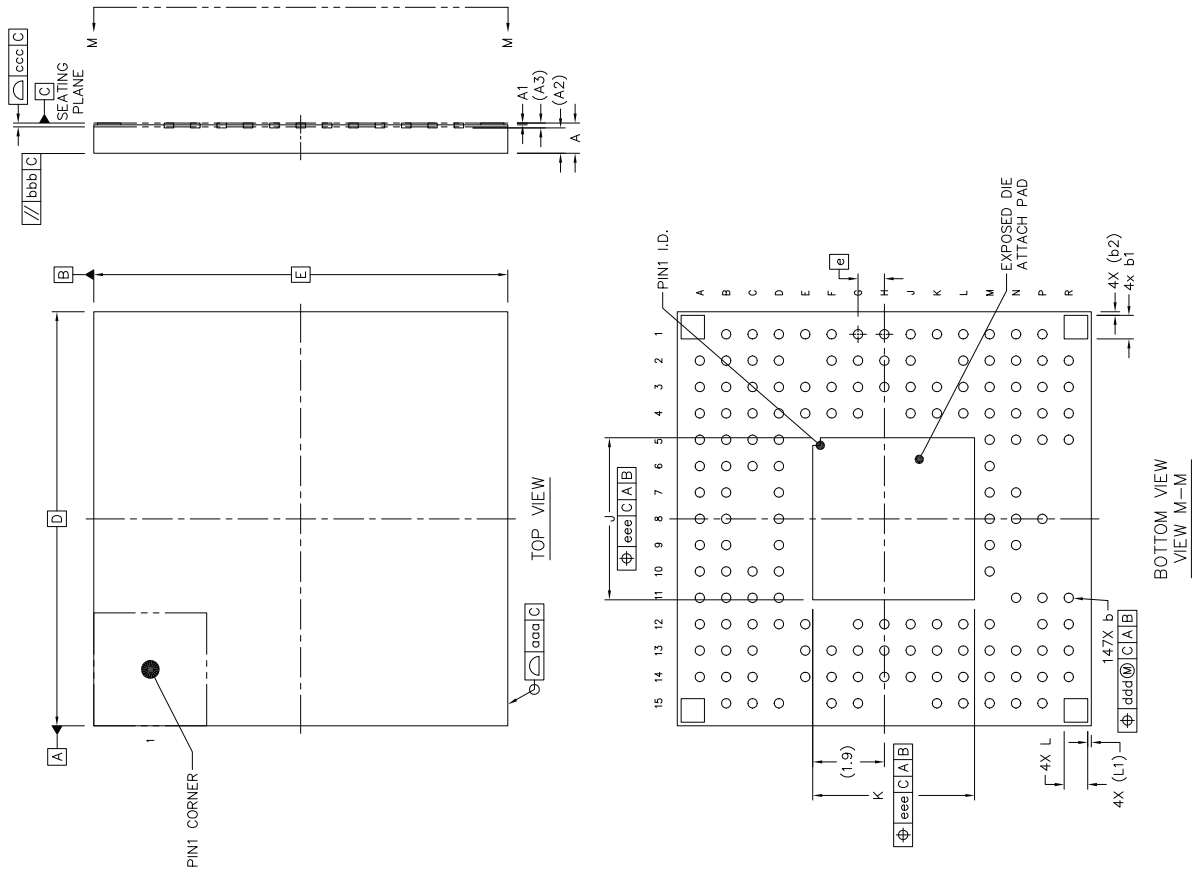

Figure 4-2: Package Dimensions aQFN 151

5.0 Temperature range

The maximum ambient temperature range for the device depends on the power consumption in the application. The power consumption mainly depends on the pixel clock frequency and the line driver settings for the cable.

Package	Power consumption	Temperature range
aQFN151	<= 0.7 W	-40°C to +105°C
	> 0.7 W	-40°C to +95°C

Table 5-1: Temperature range

6.0 Ordering Information

Device Ordering Code	Package	Quality	HDCP	Minimum Order Quantity
INAP560TAQ-T	aQFN-151	AEC-Q100	no	176 / tray
INAP590TAQ-T	aQFN-151	AEC-Q100	yes	176 / tray
INAP560TAQ-R2	aQFN-151	AEC-Q100	no	2000 / reel
INAP590TAQ-R2	aQFN-151	AEC-Q100	yes	2000 / reel

Table 6-1: Ordering information

7.0 Revision History

Revision	Date	Changes
0.1	March 2015	Initial Release
0.2	April 2015	• Added MII functionality, Updated Table 4-2, “Pin list aQFN 151” • Updated Table 3-7, “General IO Characteristics”
0.3	June 2015	• Updated Figure 4-1 "Pinout Diagram", removed pin F12 • Updated Table 4-1, “Boot-strap options”, added BST_VDD, updated BST_MII • Updated Table 4-2, “Pin list aQFN 151”, HDMI_MON needs to be left open • Updated Figure 4-2 "Package Dimensions aQFN 151" • Added Table 6-1, “Ordering information”
0.4	Oct. 2015	• Added pin SPI_M_STALL to Table 4-2, “Pin list aQFN 151” • Updated Table 4-2, “Pin list aQFN 151”, Pin REXT • Added Table 4-3, “Reset state of all digital IO pins” • Updated Table 3-3, “Supply currents” • Added INAP590T product version
0.5	Feb. 2016	• Updated temperature range from -40°C to +105°C • Updated Table 4-2, “Pin list aQFN 151” • Updated Figure 4-1 "Pinout Diagram" • Updated Figure 4-2 "Package Dimensions aQFN 151"
1.0	April 2017	• Updated Table 3-1, “Absolute maximum ratings” • Updated Table 3-3, “Supply currents” • Updated Table 3-4, “Downstream interface characteristics (TXDN0_P, TXDN0_N)” • Added Section 3.4.3.2 "SPI Slave Interface timing" • Added Section 3.4.3.3 "SPI Master Interface timing" • Added Section 3.4.3.4 "MII Interface Timings" • Added Section 3.4.3.5 "APFlag Interface" • Added Section 3.4.3.6 "I2S Audio Interface" • Added Section 5.0 "Temperature range"
1.1	May 2017	• Updated Table 3-1, “Absolute maximum ratings” • Updated Figure 3-3 "SPI Slave Timing Diagram" • Updated Table 3-8, “SPI Slave Interface characteristics”

Table 7-1: Revision History

Inova Semiconductors GmbH
Grafinger Str. 26
D-81671 Munich / Germany
Phone: +49 (0)89 / 45 74 75 - 60
Fax: +49 (0)89 / 45 74 75 - 88
Email: info@inova-semiconductors.de
URL: http://www.inova-semiconductors.com

Errata for UM_INAP560T, Rev 1.0

Order ID:
ER_UM_INAP560R_1_0
May 2019
Revision 1.1

Scope

This errata describes information to be added, changed or replaced in the INAP560T Rev1.1 user manual.

1.0 Document Updates

The following information need to be updated in the document

5.3.3 Startup procedure

The following registers access must be performed to activate and optimize the HDMI interface.

Access	Page	Address	Value	Description
W	**0x07**	**0x85**		**Set frequency range according to pixel clock 0x00: 25 - 50 MHz 0x01: 50 - 100 MHz 0x02: 100 - 200 MHz**
W	0x07	0x001	0x00	Disable parameter check (mandatory)
W	0x07	0x082	0x68	PCU command to set HDMI interrupt mask to HDMI and DVI
W	0x07	0x083	0x06	
W	0x07	0x084	0x05	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x30**	**PCU command to configure HDMI Charge pump**
W	**0x07**	**0x083**	**0xBE**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x0F**	**PCU command to configure HDMI VCO Gain**
W	**0x07**	**0x083**	**0xBF**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x02**	**PCU command to configure HDMI Band gap reference**
W	**0x07**	**0x083**	**0xC6**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	0x07	0x080	0x01	Set 5V Hot plug detect

Table 1-1: HDMI startup procedure

4.3.2 Control registers

For APIX2 upstream operation tx1_up_enable needs to be set in the PHY power down control registers. Please refer to Table 4-6 for register details.

To achieve the optimal upstream sensitivty, the upstream offset compensation must be enabled by the following register.

Addr.	Name	Bit	Default	Recommended	Self clearing	Description
0x139	**tx1_upRX_offset_enable**	**0**	**0**	**1**	**no**	**Enable upstream receiver offset compensation**

Table 4-11: Upstream offset compensation

14.7.2 PHY control registers

Table 14-21: Page 0x08, PHY control registers needs to be updated to the following description.

Addr.	Name	Bit	Default	Recommended	Self clearing	Description
0x139	tx1_upRX_calib_en	7	0	0	no	Enable upstream receiver calibration
	tx1_upRX_comp_clk	6	1	1	yes	Trigger replica gain detector comparator (compare at fallin gedge, output available at rising edge)
	tx1_upRX_comp_enable	5	0	0	no	Enable upstream receiver replica gain detector
	tx1_upRX_comp_select[1:0]	4:3	11	11	no	Select comparator input 00: Shorted input (self calibration) 01: Replica gain detector 10: Upstream Receiver with shorted input) 11: Upstream operation
	unused	2:1	00	00	no	
	tx1_upRX_offset_enable	**0**	**0**	**1**	**no**	**Enable upstream receiver offset compensation**

Table 14-21: Page 8, PHY control registers

2.0 Release History

Version	Description
1.0	Initial Release
1.1	Added Updates for 4.3.2 Control registers Added Updates for Table 14-21 Page 8, PHY control registers

Table 2-1: Release History

Inova Semiconductors GmbH
Grafinger Str. 26
D-81671 Munich / Germany
Phone: +49 (0)89 / 45 74 75 - 60
Fax: +49 (0)89 / 45 74 75 - 88
Email: info@inova-semiconductors.de
URL: http://www.inova-semiconductors.com

Errata for UM_INAP590T, Rev 1.1

Order ID:
ER_UM_INAP590R_1_1
May 2019
Revision 1.1

Scope

This errata describes information to be added, changed or replaced in the INAP590T Rev1.1 user manual.

1.0 Document Updates

The following information need to be updated in the document

5.3.3 Startup procedure

The following registers access must be performed to activate and optimize the HDMI interface.

Access	Page	Address	Value	Description
W	**0x07**	**0x85**		**Set frequency range according to pixel clock 0x00: 25 - 50 MHz 0x01: 50 - 100 MHz 0x02: 100 - 200 MHz**
W	0x07	0x001	0x00	Disable parameter check (mandatory)
W	0x07	0x082	0x68	PCU command to set HDMI interrupt mask to HDMI and DVI
W	0x07	0x083	0x06	
W	0x07	0x084	0x05	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x30**	**PCU command to configure HDMI Charge pump**
W	**0x07**	**0x083**	**0xBE**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x0F**	**PCU command to configure HDMI VCO Gain**
W	**0x07**	**0x083**	**0xBF**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	**0x07**	**0x082**	**0x02**	**PCU command to configure HDMI Band gap reference**
W	**0x07**	**0x083**	**0xC6**	
W	**0x07**	**0x084**	**0x05**	
RC	**0x07**	**0x100**		**Read clear until Bit0 = 1, hdmi_pcu_agency_done**
W	0x07	0x080	0x01	Set 5V Hot plug detect

Table 1-1: HDMI startup procedure

4.3.2 Control registers

For APIX2 upstream operation tx1_up_enable needs to be set in the PHY power down control registers. Please refer to Table 4-6 for register details.

To achieve the optimal upstream sensitivty, the upstream offset compensation must be enabled by the following register.

Addr.	Name	Bit	Default	Recommended	Self clearing	Description
0x139	**tx1_upRX_offset_enable**	**0**	**0**	**1**	**no**	**Enable upstream receiver offset compensation**

Table 4-11: Upstream offset compensation

15.8.2 PHY control registers

Table 15-32: Page 0x08, PHY control registers needs to be updated to the following description.

Addr.	Name	Bit	Default	Recommended	Self clearing	Description
0x139	tx1_upRX_calib_en	7	0	0	no	Enable upstream receiver calibration
	tx1_upRX_comp_clk	6	1	1	yes	Trigger replica gain detector comparator (compare at fallin gedge, output available at rising edge)
	tx1_upRX_comp_enable	5	0	0	no	Enable upstream receiver replica gain detector
	tx1_upRX_comp_select[1:0]	4:3	11	11	no	Select comparator input 00: Shorted input (self calibration) 01: Replica gain detector 10: Upstream Receiver with shorted input) 11: Upstream operation
	unused	2:1	00	00	no	
	tx1_upRX_offset_enable	**0**	**0**	**1**	**no**	**Enable upstream receiver offset compensation**

Table 15-32: Page 8, PHY control registers

2.0 Release History

Version	Description
1.0	Initial Release
1.1	Added Updates for 4.3.2 Control registers Added Updates for Table 15-32 Page 8, PHY control registers

Table 2-1: Release History

Inova Semiconductors GmbH
Grafinger Str. 26
D-81671 Munich / Germany
Phone: +49 (0)89 / 45 74 75 - 60
Fax: +49 (0)89 / 45 74 75 - 88
Email: info@inova-semiconductors.de
URL: http://www.inova-semiconductors.com